Design and Development of Digital Control Strategy for Solar Photovoltaic Inverter to Improve Power Quality

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Abstract: The design and development of control circuit for a solar fed cascaded multilevel inverter is postulated in this paper. The control circuit based on logic operations reduces the semiconductor switches required for the multilevel inverter. In addition to the reduction of switches, it also improves the quality of the output power by minimizing the Total Harmonic Distortion (THD). The proposed design achieves the maximum output voltage levels without the requirement of detailed look up table, boost converters and output transformers. The implementation of multilevel inverter is carriedout with asymmetrical DC sources from solar photovoltaics to achieve 2^{ns+1}-1 and 3^{ns} levels, where ns is the number of individual inverter stages. Based on the proposed design 12 switches are required to achieve 15 and 27 levels respectively, whereas the conventional inverter can able to produce only 7 levels. MATLAB/Simulink is used for the simulation of the system. The modelling of solar panel which adheres to the experimental setup is developed. A 3kWp solar plant is taken into consideration for the implementation of the proposed control design and the performance parameters are measured using power quality analyser. The results are compared with the conventional inverter which shows that the proposed inverter is much suitable for both standalone and grid connected systems.

Keywords: Digital Control, Embedded System, Multilevel Inverter, Solar Photovoltaic's, Total Harmonic Distortion

1. INTRODUCTION

Multilevel converters are finding increased attention in industry and commercial sectors as the preferred choices of electrical power conversion for medium and high power applications. There are many applications for Multi Level Inverters (MLIs), such as Flexible AC Transmission System (FACTS) equipment dealt by (Song and Liu, 2009), High Voltage Direct Current (HVDC) lines exhibited by (Flourentzou et al., 2009) and electrical drives manifested by (Hagiwara et al., 2010). (Kouro et al., 2010) conveyed that MLIs are currently commercialized in standard and customized products that power a wide range of applications, such as compressors, extruders, pumps, fans, grinding mills, rolling mills, conveyors, crushers, blast furnace blowers, gas turbine starters, mixers, mine hoists, reactive power compensation, marine propulsion, hydro pumped storage, wind energy conversion and railway traction.

Among the various MLI topologies, cascade configuration has been utilized for medium voltage and high voltage renewable energy systems such as solar Photo Voltaic (PV) due to its modular and simple structure. Application of the Cascaded Multilevel Inverter (CMLI) for renewable energy systems is reviewed by (Kjaer et al., 2005; Carrasco et al., 2006). Cascaded inverters are ideal for connecting renewable energy sources with an AC grid, because of the need for separate DC sources. This is the case in regard to applications such as solar PV or fuel cells. (Nasurudin, 2010; Jeyraj, 2009) investigated a Pulse Width Modulation (PWM) based five level CMLI and (Nasrudin et al., 2011) prescribed a seven level CMLI for PV systems with multiple reference signals. The drawback of these methods is in the requirement of complicated auxiliary circuit comprises of diodes and the need of boost converters. (Pedro et al., 2006) addressed a five level current MLI topology for single phase grid connected PV systems. The disadvantage of this method lies in the redesign of LC output filter for high power levels to reduce the physical volume of inductor and resistive losses. A five level inverter with three control loop Maximum Power Point (MPP) is proposed in (Elena et al., 2009) where an output transformer is employed between inverter and grid whereas a nine level CMLI with fuzzy logic control is implemented in (Carlo et al., 2006). This method is illustrated with input DC sources without solar panels.

Compared with Neutal Point Clamped (NPC) and Flying Capacitor (FC) MLIs, Cascaded Multilevel Inverter (CMLI) requires the least number of components to achieve the same number of voltage levels. Optimized circuit layout and packaging are possible because each level has the same structure. The only disadvantage of the CMLI is that it needs separate DC sources for real power conversions. However this disadvantage can be compensated by utilizing solar PV at its input in the proposed design. One additional advantage of

the CMLI is that if any device fails in the H-bridges, the inverter can still be operated at reduced power level. This fault tolerant configuration of CMLI was revealed by (Song and Huang, 2010; Lezana et al., 2010). Inspite of these advantages over other topologies, further reduction in the number of semiconductor devices in CMLI will certainly improve the reliability of the system. (Liu et al., 2014) found that the higher number of voltage levels can effectively decrease harmonics content of staircase output, thus significantly simplifying the output filter design.

Although switches with low voltage rating are used in a MLI, each switch requires a related gate driver circuits. This may cause the overall system to become more expensive and complex. Hence, in practical implementation, reducing the number of switches and gate driver circuits is very important. According to MIL-HDBK-217F standard quoted by (Najafi and Yatim, 2012), the reliability of the system is inversely proportional to the number of switching components. Therefore as the number of switches increases, the reliability of the converter decreases. In addition to reduction of overall reliability the efficiency of the power converter also decreases. The high number of levels increases the control complexity and introduces voltage imbalance problems. Hence it is required to improve reliability and reduce voltage imbalance for a MLI while increasing the number of output voltage levels.

To reduce the number of switching devices, the series connection of MLIs is proposed by (Kangarlu and Babaei, 2013). The disadvantage of this method is the necessary to change voltage polarity in every half cycle and also the need of switches with different voltage ratings which restrict their use in high power applications. The series connection of a high voltage diode clamped inverter and a low voltage conventional inverter is presented by (Nami et al., 2011) which require a detailed look up table. The method given by (Mondal et al., 2007) comprises two numbers of two level and three level inverters which can generate only five output levels with four DC sources, while conventional MLIs can generate upto nine levels with the same number of power supplies. The various methods for the reduction of switches proposed by (Babaei 2008, 2010; Babaei et al., 2014) require bidirectional switches with the ability to block the voltage and current in both the directions and each bidirectional switch requires a gate drive circuit which increases the power loss. Moreover umpteen works cited are implemented only with low power DC sources and switching sequence is governed by PWM techniques.

In this paper a digital logic control circuit is presented for a fifteen level (binary) and twenty seven level (trinary) solar fed cascaded multilevel inverter to achieve higher number of levels with reduced switching devices without the usage of transformer, filter components, bidirectional switches, front end rectifiers and detailed look up tables.

The paper is organized as follows: Section II presents proposed logic circuit design and Section III exhibits the simulation results and comparative analysis. Section IV presents the experimental results and Section V gives the final conclusions.

2. DIGITAL CONTROL STRATEGY

In the conventional approach, PWM techniques are used by making a comparison of reference and carrier signals to provide the required gating signals for the inverter switches. The number of output voltage levels obtained from this approach is given in the equation (1).

$$m = 2ns + 1 \tag{1}$$

where m denotes the output voltage levels and ns is the individual inverter stages. Each stage comprises of four semiconductor switches. The number of switches (l) required to achieve m levels is given in the equation (2).

$$l = 2(m - 1) \tag{2}$$

As in the case of CMLI, for the implementation of a fifteen level inverter, the number of switches required is 28 with seven individual inverter stages. In addition to the 28 switches, 182 clamping diodes are needed in NPC which is also referred as diode clamped inverter. With 28 switching devices, 91 balancing capacitors along with 14 DC bus capacitors are needed as in the case of FC to achieve fifteen level output. Increasing the number of levels will subsequently reduce the harmonic distortion which in turn improves the power quality in addition to the improvement of system reliability.

In binary mode operation, the number of levels which can be achieved for the given set of inverter stages is given in the equation (3).

$$m = 2^{ns+1} - 1 \tag{3}$$

Hence to obtain a fifteen level output, only three inverter stages are required with 12 switches. To achieve this, a switching circuit with the control strategy incorporating digital logic functions is implemented for the solar fed cascaded multilevel inverter. The three inverter stages are fed from varying solar PV input source. (Zambra et al., 2010) have compared symmetric and asymmetric CMLI and found that the latter provides higher efficiency.

Figure 1 shows the solar fed three stage CMLI power circuit which is capable of generating seven levels in conventional method, whereas the same circuit is used to achieve fifteen levels by digital switching strategy. The input voltages are scaled to the power of 2 in order to achieve the output voltage in the range of 2^{ns} which can be made possible by binary counters. An incremental and descended operator is essential to achieve the required condition given in equation (3) at the output level. For the circuit shown in Figure 1, during the positive half cycle the switches S1, S5 and S9 are in ON condition and during negative half cycle S3, S7 and S11 are in ON condition. The conduction period for each half cycle is fixed at 10ms which will determine the output frequency of the inverter as 50Hz.

The sequence shown in Table 1 gives the switching pattern to attain the desired voltage levels. IN1, IN2 and IN3 specify the three inverter stages and V_o, the output voltage. ‘0’ and ‘1’ denotes the ‘ON’ and ‘OFF’ condition of the switches. The sequence ‘001’ to ‘111’ in the positive half cycle shows

the conduction period from 0^0 to 90^0 and '111' to '001' from 90^0 to 180^0 and similar condition holds for negative half cycle from 180^0 to 270^0 and 270^0 to 360^0. The switches present in the CMLI are intended to operate based on the switching sequence enlisted in the truth table to achieve the fifteen level output. The input voltage for the first inverter stage is considered as 48V. Subsequently the other stages are scaled to the power of 2 as 48x2= 96V and 96x2=192V.

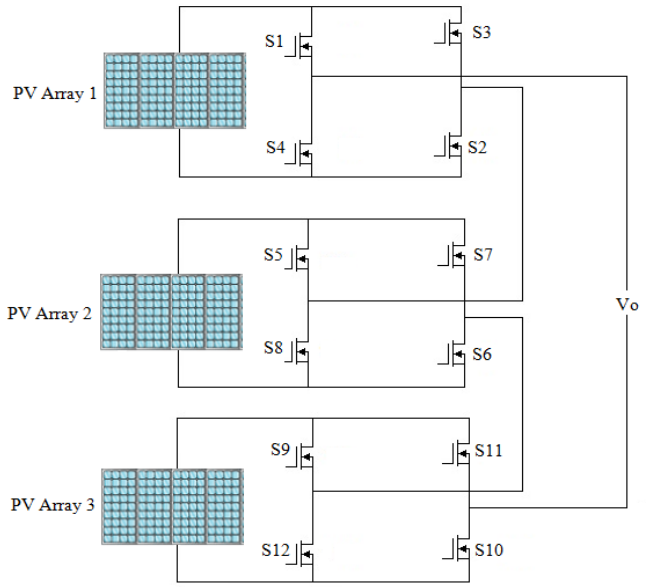

Fig. 1. Three stage inverter power circuit.

Based on the sequence given in Table 1, the first condition [0 0 1] results in arriving the output voltage with magnitude 48V square pulse in the positive half cycle. Similarly, [0 1 0] results in the output voltage with magnitude 48V+48V=96V and the other sequences continue in the same manner for obtaining the required 336V at [1 1 1] upto the first half of the positive cycle. This operation requires the bits to move towards the forward direction from 0^0 to 45^0. The next half of the positive cycle is completed by reversing the above sequence from [1 1 1] to [0 0 1] making the bits to move towards the opposite direction from 45^0 to 90^0. Again during the negative half cycle the sequence is repeated in the same manner.

Figure 2 shows the block diagram for the implementation of the binary mode. The power switches in the inverter are operated in a sequence resembling the truth table of a counter. Thus for implementing a CMLI with firing sequence requirements, it requires N_s+2 bit counters. The three stage inverter requires N_s+2 (3+2=5) bit counters which acts as an up counter. The combinational logic circuit makes the three bits (Q1, Q2 and Q3) to move in forward direction during the first half of the positive half cycle and similarly in reverse direction during second half of the positive half cycle.

The same condition is repeated in both half of the negative half cycle. The bits (Q1, Q2 and Q3) are modified by Q4 and Q4', where Q4'is used to control the incremental operation in the first half of positive or negative half cycles and Q4 is used for the decrement operation in the latter half of positive or negative half cycles. The pulse separation block comprises of bits Q5' and Q5 to separate the pulses required for both positive and negative half cycles and also controls other bits in the circuit. The detailed layout of the proposed methodology is shown in Figure 3 in which 'n' denotes the number of individual inverter stages.

Table 1. ON/OFF states for inverter switches

Positive Half cycle (10ms)				Negative Half cycle (10ms)			
IN3	IN2	IN1	V_o	IN3	IN2	IN1	V_o
0	0	1	48	0	0	1	-48
0	1	0	96	0	1	0	-96
0	1	1	144	0	1	1	-144
1	0	0	192	1	0	0	-192
1	0	1	240	1	0	1	-240
1	1	0	288	1	1	0	-288
1	1	1	336	1	1	1	-336
1	1	1	336	1	1	1	-336
1	1	0	288	1	1	0	-288
1	0	1	240	1	0	1	-240
1	0	0	192	1	0	0	-192
0	1	1	144	0	1	1	-144
0	1	0	96	0	1	0	-96
0	0	1	48	0	0	1	-48

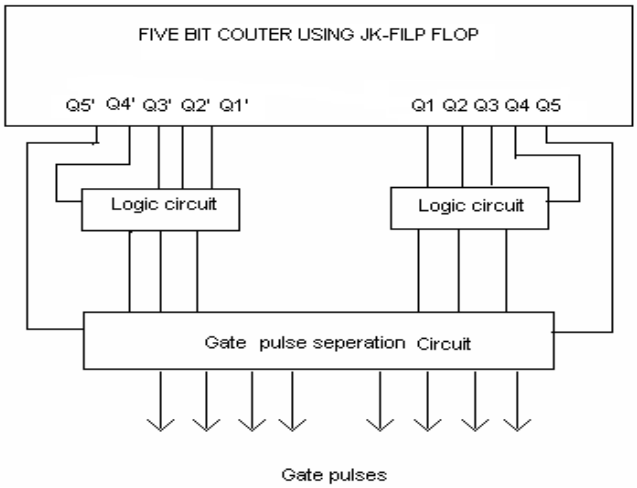

Fig. 2. Block diagram of the logic circuit.

Figure 4 shows the output waveform of fifteen level inverter in which level 1 is achieved at origin and level 2 to level 8 illustrates the 7 voltage steps achieved in positive half cycle marked as "7V". A similar conduction holds for the negative half cycle from level 9 to level 15 in which the remaining 7 voltage steps tend to "-7V". The inverter with higher voltage level (4V) has a lower number of commutations and thereby reduces the switching losses. Any number of levels can be achieved with this methodology by only adding the counters in accordance with the number of inverter stages and control logic functions. In the proposed methodology, instead of V_{PV1}= V, V_{PV2}= 2V and V_{PV3}= 4V as stated in Figure 4, the case V_{PV1}= 48V, V_{PV2}= 96V and V_{PV3}= 192V is considered to generate fifteen level with the output voltage of $336V_p$.

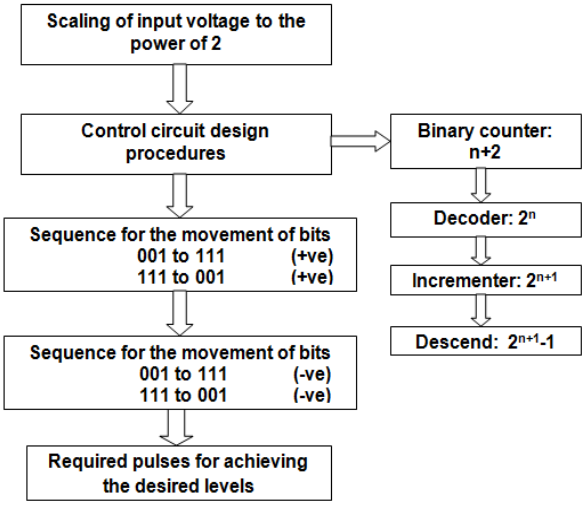

Fig. 3. Flow chart of the proposed logic design.

For the power circuit shown in Figure 1, with the three inverter stages twenty seven levels can be obtained with only 12 switches in trinary mode. This mode is referred as trinary where the input voltages are scaled to the power of 3 rather than 2 in binary mode. In trinary mode operation, the number of levels which can be achieved for the given set of inverter stages is given in the equation (4).

$$m = 3^{ns} \tag{4}$$

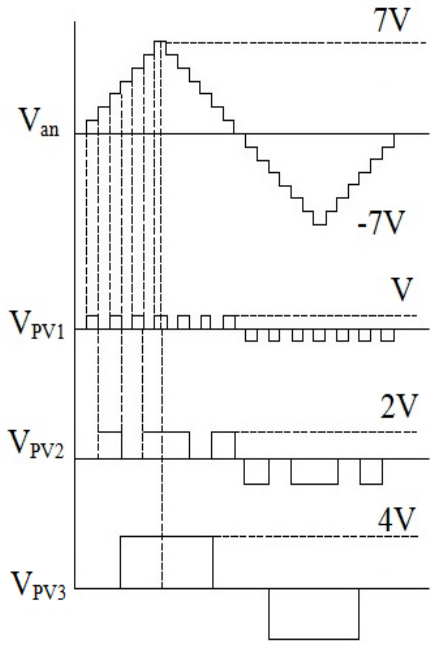

Fig. 4. Switching sequence in binary mode.

Figure 5 shows the sequence of switching for a three stage twenty seven level inverter. Table 2 illustrates the switching sequence for the switches S1 to S12 to get twenty seven level output. The sequence shown in Table 2 is given for only positive half cycle to get thirteen level and in negative half cycle the same sequence is rotated by an angle of 90^0 to achieve the remaining thirteen level. By including level zero, the desired twenty seven levels will be achieved.

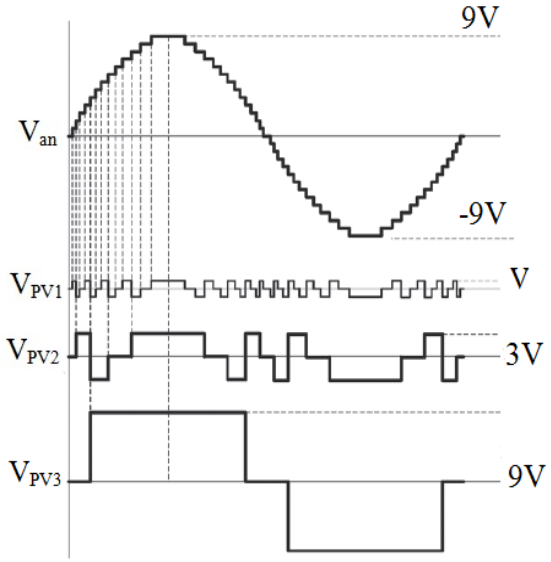

Fig. 5. Switching sequence in trinary mode.

Table 2. ON/OFF states for inverter switches

level	S1	S2	S3	S4	S5	S6
1	1	0	0	1	1	1
2	0	1	1	0	1	0
3	1	1	0	0	1	0
4	1	0	0	1	1	0
5	0	1	1	0	0	1
6	1	1	0	0	0	1
7	1	0	0	1	0	1
8	0	1	1	0	1	1
9	1	1	0	0	1	1
10	1	0	0	1	1	1
11	0	1	1	0	1	0
12	1	1	0	0	1	0
13	1	0	0	1	1	0

level	S7	S8	S9	S10	S11	S12
1	0	0	1	1	0	0
2	0	1	1	1	0	0
3	0	1	1	1	0	0
4	0	1	1	1	0	0
5	1	0	1	0	0	1
6	1	0	1	0	0	1
7	1	0	1	0	0	1
8	0	0	1	0	0	1
9	0	0	1	0	0	1
10	0	0	1	0	0	1
11	0	1	1	0	0	1
12	0	1	1	0	0	1
13	0	1	1	0	0	1

To achieve this, rather than a digital logic function used in binary mode, an embedded controller is proposed without the utlilisation of transformers and complicated algorithms which was used by (Kang et al., 2005, Dixon et al., 2007). In the trinary approach, the input voltages are scaled to the power of 3.

A three stage twenty seven level asymmetric inverter presented by (Dixon et al., 2010) requires independent power supply with high frequency link, chopper circuit, transformer with six secondary windings of turn's ratio 9:3 and diode bridge rectifier. As the transformer works on square wave, a specific design is required and the presence of transformer increases cost, space, weight and associated losses.

3. SIMULATION RESULTS

Simulations are carried out in MATLAB/Simulink 2013a. The input source for the CMLI is considered as solar PV panels which are scaled to the power of 2 and 3 for increasing the output levels. The PV panel which serves as the input source for the individual MLI stages is modelled according to the commercial PV used in the hardware implementation. One of the problems in the PV generation systems is that the amount of electric power generated by the solar arrays is always changing with weather conditions, i. e. the intensity of solar radiation. The modelled PV panel considers the variation in both temperature and irradiance by observing the real time data of these parameters for the geographic region. In order to achieve the panel of required rating, the mere consideration is focused on modelling of both solar cell and solar modules to develop a solar PV array. As the polycrystalline silicon based solar panel is used for the implementation, a double exponential model shown in Figure 6 is modelled which is derived from the physical behaviour of the solar cell constructed from polycrystalline silicon. The shunt resistance R_p is inversely related to shunt leakage current to the ground. The efficiency of PV is insensitive to the variation in R_p and the shunt leakage resistance can be assumed to approach infinity without leakage current to ground. A small variation in R_s will significantly affect the PV output power. Each panel is rated at 48V by the series connection of four numbers of 12V modules. Further series connections of two or three PV panels give the input of 96V and 192V respectively. The input voltages are in the range of 48V, 96V and 196V. The solar cell rating of V_{oc}=0.5V and I_{sc}=7A is choosen based on the datasheet of the commercial solar PV specifications.

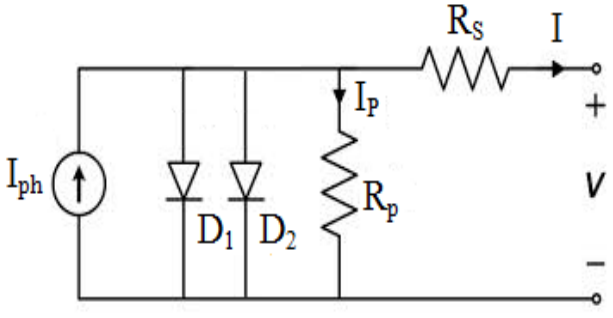

Fig. 6. Equivalent circuit of the solar cell.

Nearly 24 solar cells are connected in series at Standard Test Conditions (STC) to develop a 12V, 7A which constitutes a single solar module. Four such modules are connected in series to achieve 48V, 12A solar PV array or panel. The series connection of the module is same as that of the cell. This 48V, 7A solar PV serves as the input source for the single inverter stage. In the proposed design, seven numbers of such input sources are modelled to power the seven inverter stages, thereby a fifteen level output waveform is obtained. The following relations given in equations (5) and (6) holds good for the desired design requirements.

$$V_{peak} = 48V \times 7 = 336V \tag{5}$$

$$V_{RMS} = \frac{336}{\sqrt{2}} = 237.59V \tag{6}$$

In order to extend the system for making it suitable for grid connected system, the condition given in equation (7) need to satisfied as given by (Nasrudin, 2011).

$$V_{dc} > \sqrt{2}V_{grid} \tag{7}$$

In the proposed design, the total V_{dc}=336V which is greater than the square root of the grid voltage ($230V_{RMS}$) as per the condition given in the equation (7).

As the design made for STC, it produces the fixed DC output from solar panel without any variations. Most of the models in various literature deals with the fixed output supply panels. Hence the PV panel model which exhibits the variations thus occurring due to temperature and irradiance is required to adhere the real time specifications. In order to achieve this, a detailed analytical study is undertaken throughout the year by solar PV observatory for the geographic location where the experiment is conducted. The radiation measurements used are bean and diffuse horizontal surface radiation gathered with a PV pyranometer.

Figures 6 and 7 show the analysis which depicts the irradiation and temperature levels measured for the months of January and November. Based on the analysis it is found that the irradiance varies from 0W/mm^2 to 1000W/mm^2. The Solectric 9000 model is taken into consideration for modelling which provides 115W of nominal maximum power and it has 24 series connected polycrystalline silicon cells for a single module. It consists of two by pass diodes each of which is connected in antiparallel with 12 series connected cells are used for modelling. In order to verify the model the voltage current and power voltage characteristics are plotted as shown in Figures 8 and 9. These plots are obtained for the various irradiance levels and temperature limits. This graph clearly shows the V_{oc}, I_{sc}, V_{mpp}, I_{mp} and P_m which are the important criteria for MPP tracking. Based on the characteristics it is found that the non linear nature of PV cell is apparent. The output current and power of PV cell depend on the cell's terminal operating voltage, temperature and solar insolation. With the increase in working temperature, the I_{sc} of the PV cell increases whereas the maximum power output decreases. If the increase in the output voltage is much less than the decrease in the voltage, the net power decreases at high temperatures. The increase in solar irradiance increases I_{sc} of the PV module and the

maximum power output increases. This is due to the fact that the V_{oc} is logarithmically dependent on the solar irradiance and I_{sc} is directly proportional to the radiant intensity.

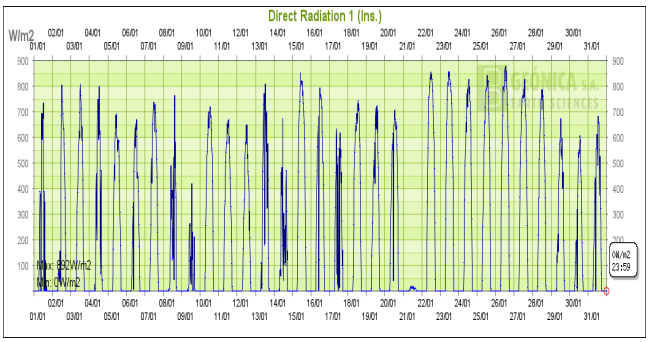

Fig. 8. Solar data for the month of January.

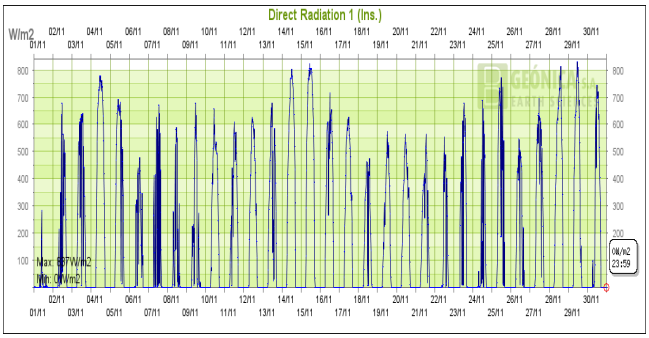

Fig. 9. Solar data for the month of November.

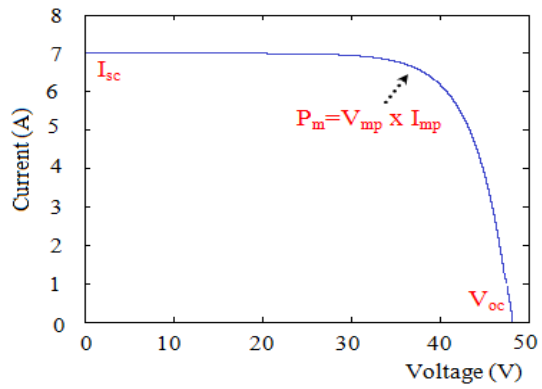

Fig. 10. V-I characteristics of solar PV array.

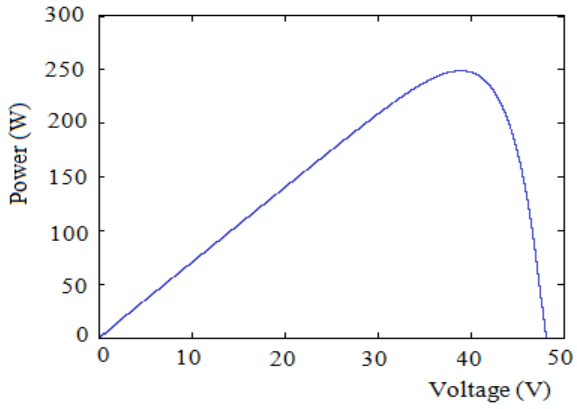

Fig. 11. V-P characteristics of solar PV array.

For the circuit shown in Figure 1, the simulation is conducted in 'binary' and 'trinary' modes. For 'binary' mode, digital switching strategy is followed and subsequently in 'trinary' mode, embedded controllers are used in accordance with the truth table.

Figures 12 and 13 shows the seven level output voltage waveform obtained from the three stage inverter for the power circuit given in Figure 1 and its corresponding THD analysis. In this simulation, conventional PWM is used to generate the gating signals for the inverter switches.

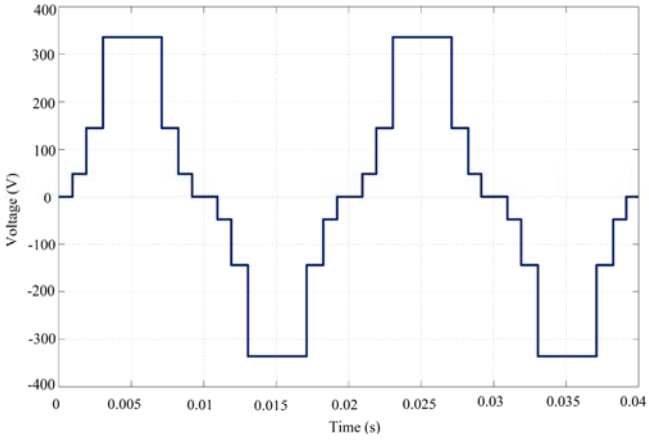

Fig. 12. Three stage seven level waveform.

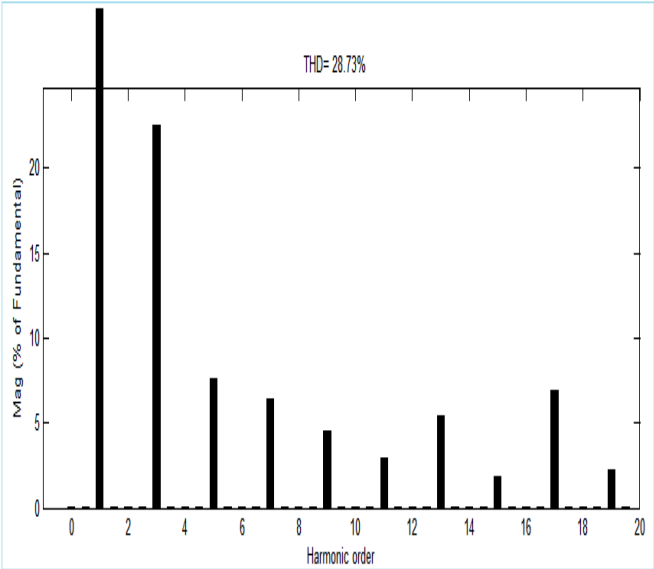

Fig. 13. FFT analysis for seven level inverter.

In 'binary' mode the input to the three inverter stages are to be scaled in the power of 2 as 48V, 96V and 192V to achieve the output voltage of $326V_p$. Figure 14 shows the proposed simulation block of the control circuit which consists of counters, combination circuit and pulse separation circuit. The clock signal is given as the input to the five bit asynchronous counter for the movement of bits suitable for positive and negative half cycles according to the truth table. At logic functions block, the pulses are separated and given to the inverter switches. Figure 15 shows the fifteen level output voltage waveform achieved from three stage inverter and its corresponding FFT analysis is given in Figure 16.

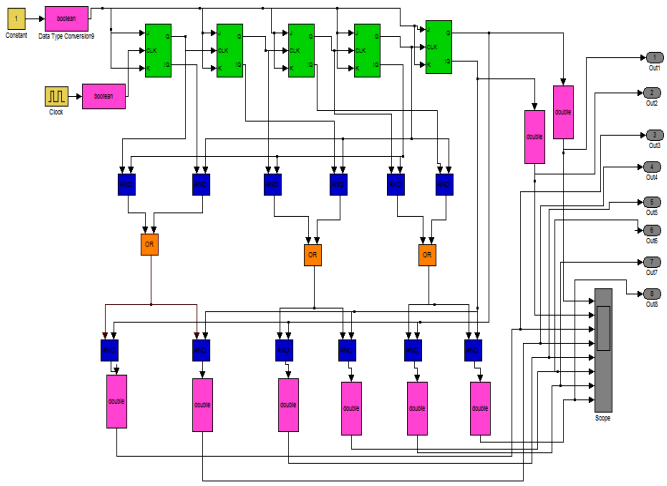

Fig. 14. Switching circuit for three stage inverter.

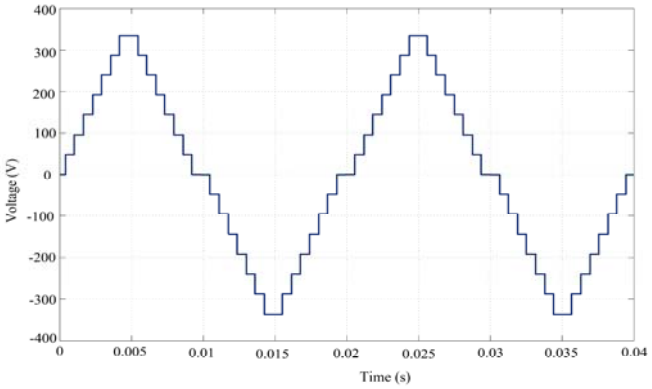

Fig. 15. Three stage fifteen level waveform.

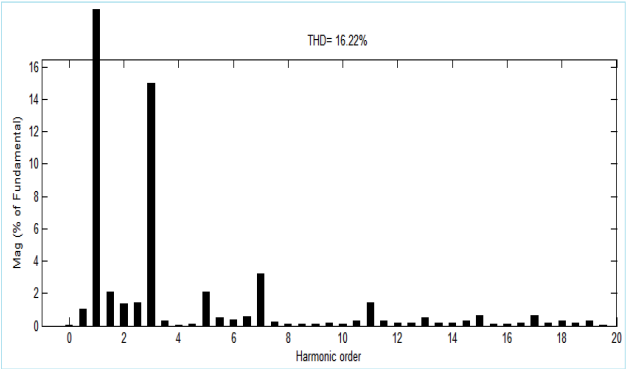

Fig. 16. FFT analysis for fifteen level inverter.

The simulation is carried out from single stage to seven stage CMLI in binary mode. With the proposed control circuit topology, the increase in levels is achieved by including an additional counter, AND gates with the multiples of four (for single stage 4 AND gate is needed and for two stage 8 AND gates) and OR gates. Figure 17 shows the 255 level output waveform achieved by seven stage CMLI. The conventional seven stage CMLI can generate only fifteen levels. In order to achieve 255 level output in conventional inverter, it requires 127 inverter stages and 508 switching devices. Figure 18 shows the variation of THD obtained for various levels.

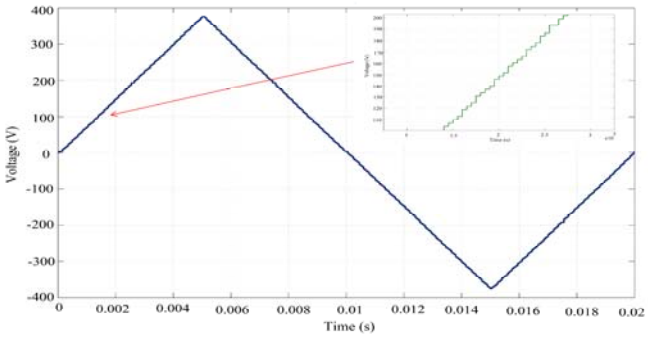

Fig.17. Seven stage 255 level waveform.

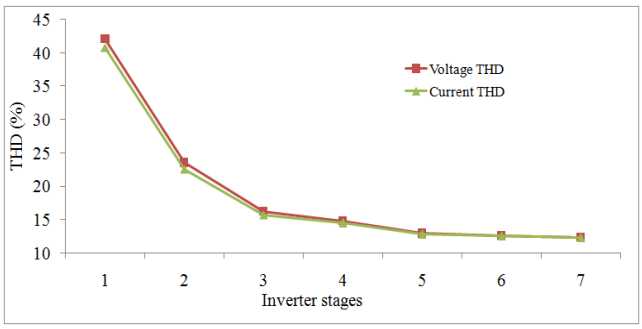

Fig. 18. Variation of THD in binary mode.

In 'trinary' mode the inputs to the three inverter stages are to be scaled in the power of 3 as 24V, 72V and 216V to achieve the output voltage of $312V_p$. An embedded controller is used which can further reduce the complexity and in this topology the levels can be achieved even greater than 1000. The truth table is incorporated into the controller which generates the suitable sequences to turn ON/OFF the semiconductor switches by repeating sequence block. Here too, any number of levels can be achieved by suitable formulation of look up table. Figure 19 shows the output voltage waveform of a 3 stage 27 level inverter and its corresponding harmonic spectrum is given in Figure 20. The variation of THD for various stages obtained by trinary mode is shown in Table 3. It is observed that while increasing the number of levels greater than 100, the values of harmonic distortions summarily increase. Hence the increase of levels can be set within the prescribed limit in proving the required improvement in power quality.

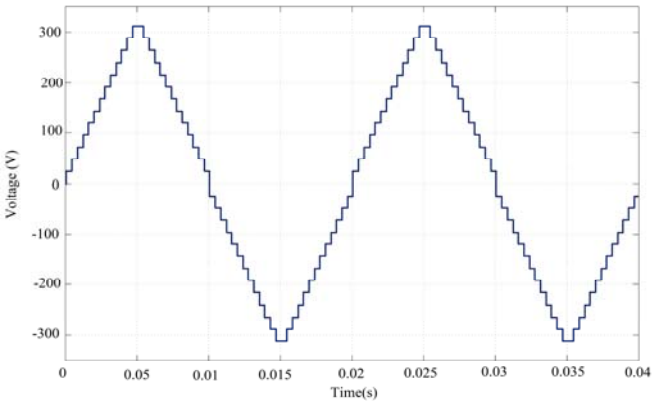

Fig. 19. Three stage 27 level waveform.

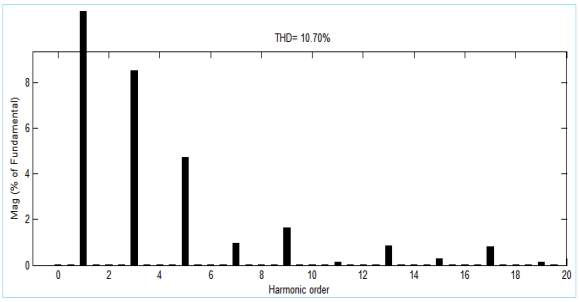

Fig . 20. FFT analysis for 27 level inverter.

Table 3. Variation of THD in trinary mode

Stages	Levels	V_{THD} (%)	I_{THD} (%)
3	27	10.70	7.71
4	81	11.37	8.66
5	243	11.77	9.00
6	729	11.76	11.96
7	2187	12.02	11.95

4. EXPERIMENT RESULTS

A 3kWp solar PV power supply unit is designed and implemented for binary and trinary topologies individually and results are obtained. In most of the countries, much of the domestic loads operate from a single phase 230V, 50Hz AC system. Hence the output voltage of the system is designed for the 230V AC supply. In order to achieve this, the input supplies are in the range of 48V, 96V and 192V (asymmetrical) respectively. Each solar PV panel has a rated power of 115W with voltage variation of 16 to 21 volts (nominal 12V) depending on the operating conditions such as light intensity, etc. Four PV modules are connected in series to get a nominal voltage of 48V which constitutes a single individual source. Four numbers of 12V, 100Ah battery packs are connected in series to get a nominal DC bus of 48V. These batteries are charged from the solar PV unit through a controlled charging circuit. There are seven sets of individual solar PV supply source used for the hardware implementation as given in equation (8). Table 4 shows the specifications of the hardware setup and the 3kWp solar PV plant is illustrated in Figure 21. The complete experimental setup is shown in Figure 22. The input from the solar PV denotes the connection link from $3kW_p$ solar plant.

$$48 + (48x2) + ((48x2)x2) = 336Vp \quad (8)$$

Fig. 21. 3kWp solar PV plant.

Table 4. Experimental setup specifications

Solar Panel Descriptions	
Model	Solectric 9000
Pmpp	115Wp
Voc	21.2V
Isc	7.4A
Vpm	16.5V
Ipm	6.95A
Max system voltage	540V
Tolerance at peak power	±5%
No. of panels	28
Total power	3220Wp
Charge Controllers (CC)	
Make	Sukaam
V-I Rating	48V,10A
No. of CC	7
Battery bank	
Make	EXIDE
Model	6LMS100L
Voltage	12V
Ampere Hour	100Ah
No. of batteries	28
Hardware Description	
Switch	MOSFET IRF840
No. of switches	12
Controller	ATMEGA 16AVR
Measuring Instruments	
Oscilloscope	Tektronix
Logic Analyser	Standard
Power Quality Analyser Make	WT 3000 Yokogawa

The protection circuit in Figure 22 comprises of switchgear components such as fuses and contactors to limit the over current entering into the inverter circuits. This block also includes the scaling of input voltages in the power of 2 and 3 to achieve binary and trinary modes of operation. By loading the sequence of switching for binary and trinary, fifteen and twenty seven levels can be obtained from the same circuit where the other component blocks remain the same.

As the control circuit is the integral part of the system, it consists of counter CD4520, IC 555, combinational circuit with logic gates and buffer IC. In order to reduce further complexity the logic is programmed in a single chip microcontroller ATMEGA 16AVR. The switching signals are generated as per the switching sequence given in the truth table. In order to make the bits to move in forward and reverse direction appropriately without any mismatch a dead

time of 1μs is introduced. The inverter shown in Figure 22 is used to achieve both 15 and 27 levels by only updating the switching patterns as per the truth table. It is considered that the inputs to the three stage inverter circuit are 48V, 96V and 192V (binary) and 24V, 72V and 216V (trinary). As the individual battery rating is of 12V, 100Ah, its series connection results in the required scaling of input voltages.

Fig. 22. Complete experimental setup.

Figures 23 and 24 shows the output voltage waveforms obtained from binary and trinary modes showing fifteen and twenty seven levels respectively. Based on the power quality analysis with WT3000, it if found that for 15 level inverter the THD=15.483% and for 27 level the THD=13.678%.

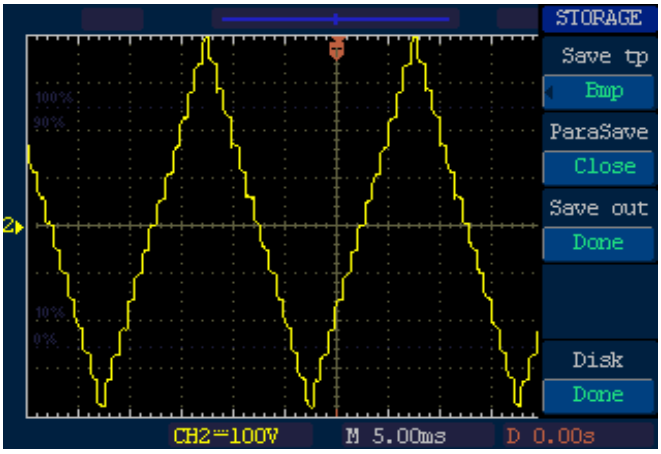

Fig. 23. Fifteen level output voltage waveform.

Table 5 shows the comparison amidst the methods opted for switches reduction. Based on the comparison its shows that the proposed design gives the significant result in improving both reliability and power quality. It is also to register that none of the methods for switches reduction is intended towards solar PV applications.

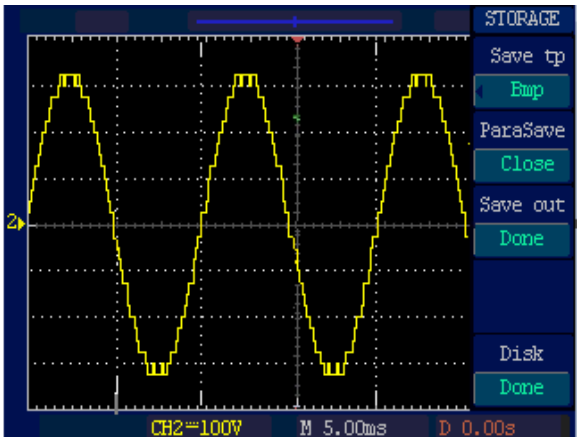

Fig. 24. Twenty seven level output voltage waveform

Table 5. Comparative analysis

Authors	Levels	Switches
Hinago and Koizumi (2010)	15	14
Nami et al. (2011)	15	19
Najafi and Yatim (2012)	15	18
Nasrudin et al. (2013)	15	18
Proposed	15 & 27	12

5. CONCLUSIONS

This paper presents the harmonic profile improvement in a solar fed cascaded multilevel inverter with the low cost digital switching circuit. In this method a three stage inverter is taken into consideration to obtain 15 and 27 levels whereas in conventional inverter only 7 levels can be achieved. The mathematical model for solar PV is carried out for providing input source to the inverter stages. The digital control method is applied to a 3kWp solar PV plant and the measurement results are analyzed. The Total Harmonic Distortion decreases with increasing the number of inverter stages. In addition the number of semiconductor devices also gets reduced without the requirement of transformers, boost choppers and detailed look up tables. This method can be implemented in a standalone/ grid interacted PV systems to improve power quality.

ACKNOWLEDGMENTS

The authors acknowledge and thank the Department of Science and Technology (Government of India) for sanctioning the research grant for the project titled, “DESIGN AND DEVELOPMENT OF MULTILEVEL INVERTERS FOR POWER QUALITY IMPROVEMENT IN RENEWABLE ENERGY SOURCES” (Ref.No.DST/TSG/NTS/2009/98) under Technology Systems Development Scheme for completing this work.

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