The Impact of Supply Voltage Reduction on The Static Noise Margins of a 6T-Sram Cell

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Abstract: The power consumption, especially the leakage power, is a big issue in nanometric technologies. In scaled technologies, the impact of lowering the supply voltage in order to ensure the low leakage power, leads to a decrease in robustness. The paper investigates the effect of lowering the supply voltage on the robustness of a 6T SRAM cell, both in saturation and sub-threshold regimes. The Static Noise Margin (SNM) is evaluated analytically and compared with HSPICE simulations for 130nm, 90nm and 65nm Berkeley Predictive Technology Models (BPTM) [9]. Our results show that the SNM of the cell decreases nonlinearly with a linear decrease in the supply voltage. The proposed analytical model is also used to predict the minimum value of the supply voltage that preserves the data stored in a 6T-SRAM cell, which is found to be approximatively 5% of the nominal value.

Keywords: SRAM memory retention, SNM estimation, leakage power

1. INTRODUCTION

Reducing the standby current, which is due to different leakage currents, is critical in low-power design. At the circuit level, leakage reduction can be achieved by controlling the voltage of different device terminals. SRAM leakage power can be effectively reduced by lowering the supply voltage (V_{DD}) to its standby limit, as indicated by Qui et al. in [1]. Reducing the supply voltage influences the cell's robustness. This robustness can be expressed in terms of immunity to noise which can be quantified as the amount of voltage noise at the internal nodes necessary to flip the cell's state, and is usually referred to as the static noise margin (SNM). The value of the minimum supply voltage that preserves the data stored in a SRAM cell provides an estimation of the maximum achievable leakage reduction for a given technology.

The paper describes a method to estimate analytically the static noise margin of 6T-SRAM cell in sub – and above – threshold regimes. The results are validated by HSPICE simulation, using Seevinck's graphical method [2]. Through the years, various methods of computing the static noise margin were proposed. Seevinck et al. in [2] and by Bhavnagarwala et al. in [3] developed expressions for above – threshold static noise margins and Calhoun and Chandrakasan [4] and Welling and Zory [5] developed expressions for sub – threshold static noise margins. In [2] the authors describe an explicit analytic expression for the static noise margin based on long channel models as a function of device parameters and supply voltage. Bhavnagarwala et al. [3] studies the SRAM cell static noise margin reduction due to intrinsic threshold voltage fluctuations in uniformly doped minimum geometry MOSFETs. The work described in [5] investigates stability aspects of sub-threshold SRAM cells, deriving analytical expressions for the SNM as a function of circuit parameters, operating conditions and process variations. The noise margin of SRAM cells in low power conditions such as low supply voltage and source-body bias is experimentally determined, using a graphical approach in Cseveny et al. [6] and Hook et al. [8]. Calhoun and Chandrakasan [4] analyse the dependence of SNM on supply voltage, temperature, transistor sizes and global process variation in a commercial 65nm technology.

This paper builds on previous work examining the influence of lowering the supply voltage of a SRAM cell on its robustness (noise immunity), both in above– as in sub–threshold regions taking into account the short channel effects in MOSFET scaling, as velocity saturation and channel length modulation. The result of channel length modulation is an increase in current due to Short Channel Effects (SCE) when the Drain-Source voltage increases.

The following section of the paper presents a method to model the SNM of a 6T SRAM cell in low power mode and the model validation by comparing the results to the ones obtained with HSPICE simulations for 130nm, 90nm and 65nm BPTM [9]. Also, based on this model, the minimum supply voltage ($V_{DD\text{-}min}$) that preserves the data stored in a SRAM cell is estimated.

2. STATIC NOISE MARGIN IN LOW LEAKAGE POWER MODE

A SRAM cell's immunity to static noise is normally expressed in terms of Static Noise Margin (SNM) which quantifies the amount of voltage noise necessary to flip the cell's contents.

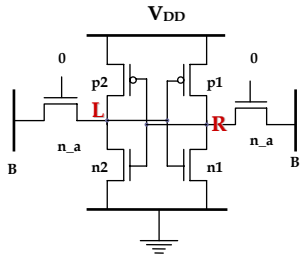

Fig.1.Conventional 6T SRAM cell in standby

The circuit diagram of a 6T SRAM cell in standby is illustrated in Figure 1. This cell can be also represented by a flip-flop consisting of two inverters as shown in Figure 2 given that in standby the access transistors are off. The voltage sources V_{n1} and V_{n2} in Figure 2 represent the static noise in the circuit. The maximum noise level that can be tolerated by the flip-flop before switching states defines the *static noise margin* (SNM) [2].

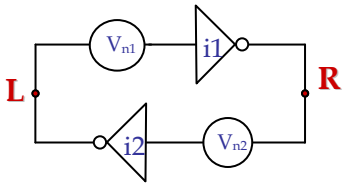

Fig. 2.Cell consisting of two inverters and noise sources

Graphically, the SNM of the 6T-SRAM cell can be estimated by drawing the voltage transfer characteristics (the DC input-output characteristic) of the two inverters obtaining the so called "butterfly curve" and finding the maximum possible square between them [2] as illustrated in Figure 3.

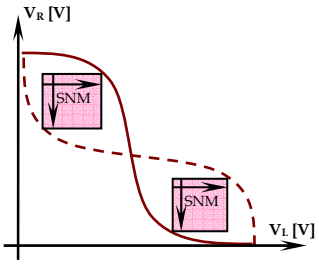

Fig. 3. Graphical representation of SNM

From these curves the main circuit characteristics can be extracted: the output voltages V_{OH} (highest output voltage – max(V_{out})) and V_{OL} (lowest output voltage – min(V_{out})), the input voltages V_{IH} (the smallest value of the input voltage that can be interpreted as logic 1) and V_{IL} (the largest value of the input voltage that can be interpreted as logic 0), and the inverter threshold V_M. By definition, V_{IL} and V_{IH} are the operation points for which the slope of VTC is -1.

The models proposed in this paper have the same starting point: Kirchhoff's current law (taking into account the drain current) applied on the "L" and "R" nodes of the memory cell as indicate in Fig. 1. The drain current, I_D, in saturation and sub-threshold, is given in [7] and it has the expression:

$$I_{D,sat} = kV_{DSAT}\left(V_{GS} - V_{TH} - \frac{V_{DSAT}}{2}\right)\cdot (1+\lambda V_{DS}) \quad (a)$$

$$I_{D,sub-th} = I_S \exp\left(\frac{V_{GS}}{nV_T}\right)\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right)\cdot (1+\lambda V_{DS}) \quad (b) \qquad (1)$$

Equation (1a) gives the expression of the drain current ($I_{D,sat}$) when the velocity saturation is achieved ($V_{DS} \geq V_{DSAT}$). In this equation, k, defined by (2), is the transistor's gain, V_{DSAT}, defined by (3), is the velocity saturation voltage, V_{TH} is the threshold voltage bias dependent and λ is the channel length modulation coefficient.

$$k = \frac{\mu\varepsilon_{ox}}{t_{ox}}\cdot\frac{W}{L} \qquad (2)$$

$$V_{DSAT} \approx \frac{Lv_{sat}}{\mu} \qquad (3)$$

(W – channel width, L – channel length, μ – carrier mobility (electrons or holes); ε_{ox} – gate dielectric constant, t_{ox} – gate oxide thickness, v_{sat} – carrier (electrons or holes) saturation velocity). Equation (1b) gives the expression of the drain current ($I_{D,sub-th}$) in the sub-threshold regime ($V_{GS} < V_{TH}$). In this equation I_S is the current when $V_{GS} = V_{TH}$, n is the sub-threshold swing coefficient and V_T is the thermal voltage. The term $1+\lambda V_{DS}$ in (1) is a correction introduced to model the short channel effect (SCE).

2.1. Modeling SNM in Saturation Region

The voltage transfer characteristic (VTC) of the CMOS inverter in above-threshold region has a very slim transition region in which, a small change of the input voltage will lead to an important change in the output voltage. In this case, the critical output voltages are: $V_{OH} = V_{DD}$ and $V_{OL} = 0V$. A relative simple method to approximate the noise margins is given by Rabaey et al. in [7]. The authors use a piecewise linear approximation of the voltage transfer characteristic, as illustrated in fig. 4 (a).

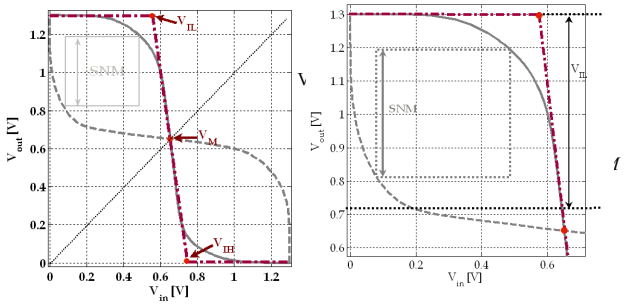

Fig. 4. (a) Piecewise linear approximation of the VTC, (b) First order correction in SNM estimation

The transition region is approximated by a straight line that has the same slope (g) as the transfer characteristic in the commutation point (V_M). The noise margins are defined as

the intersections of the tangent to the VTC in V_M with V_{DD} and 0 respectively (see figure 4a):

$$SNM_L = V_{IL} = V_M + \frac{V_{DD} - V_M}{g} \tag{4}$$

$$SNM_H = V_{DD} - V_{IH} = V_{DD} - V_M\left(1 - \frac{1}{g}\right) \tag{5}$$

The commutation threshold (V_M) is the point where $V_{in} = V_{out}$. Its value can be graphically determined as the intersection between the voltage transfer characteristic and the line given by $V_{in} = V_{out}$. Also, this point can be analytically determined from the current law, considering that in this region the transistors are both saturated (1a) and the currents are equal with opposite signs:

$$I_{DSn} + I_{DSp} = 0 \tag{6}$$

$$I_{DSn} = k_n V_{DSATn}\left(V_{in} - V_{THn} - \frac{V_{DSATn}}{2}\right)\left(1 + \lambda_n V_{out}\right) \tag{7}$$

$$I_{DSp} = k_p V_{DSATp}\left(V_{in} - V_{DD} - V_{THp} - \frac{V_{DSATp}}{2}\right)\cdot \cdot\left(1 + \lambda_p V_{out} - \lambda_p V_{DD}\right) \tag{8}$$

and $V_{in} = V_{out} = V_M$.

The commutation threshold depends on the ratio between the widths and lengths of the two transistors ((6) ÷ (8)). In order to obtain symmetry, a balanced memory cell has assumed. In this case the $(W/L)_p$ to $(W/L)_n$ ratio is chosen by design so that the commutation threshold is half of the supply voltage ($V_M = V_{DD}/2$).

The slope of the VTC is obtained differentiating (6) ÷ (8):

$$g = \frac{dV_{out}}{dV_{in}} = \tag{9}$$

$$= \frac{c_n(1 + \lambda_n V_{out}) + c_p\left[1 + \lambda_p(V_{out} - V_{DD})\right]}{\lambda_n c_n\left(V_{in} - V_{THn} - \frac{V_{DSATn}}{2}\right) + \lambda_p c_p\left(V_{in} - V_{DD} - V_{THp} - \frac{V_{DSATp}}{2}\right)}$$

where $c_n = k_n V_{DSATn}$ and $c_p = k_p V_{DSATp}$. And making $V_{in} = V_{out} = V_M = V_{DD}/2$ we obtain the slope as a function of supply voltage $g(V_{DD})$.

Because the inverter is dimensioned so that $V_M = V_{DD}/2$, the noise margins defined by (4) and (5) are equal and their dependence on the supply voltage is given by:

$$SNM_L = SNM_H = V_{IL} = \frac{V_{DD}}{2}\left(1 + \frac{1}{g(V_{DD})}\right) \tag{10}$$

Since by definition, V_{IL} and V_{IH} are the operation points for which the slope of VTC is -1, we introduce a correction to this model in order to achieve a better estimation of the noise margin (fig. 4b):

$$SNM = V_{IL}(V_{DD}) - d \tag{11}$$

To determine the value of d, the segment AC of the VTC is approximated as a second order function: $V_{out} = aV_{in}^2 + bV_{in} + c$. The constants a, b and c can be computed by imposing three conditions:

- the characteristic passes by point A(V_{TH},V_{DD})
- the characteristic's slope at point A is 0
- the characteristic's slope at point C(V_{IL},V_{out}) is -1

The following system of equations was obtained:

$$\begin{bmatrix} V_{TH}^2 & V_{TH} & 1 \\ 2V_{TH} & 1 & 0 \\ 2V_{IL} & 1 & 0 \end{bmatrix}\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} V_{DD} \\ 0 \\ -1 \end{bmatrix} \tag{12}$$

with the solutions:

$$\begin{cases} a = \dfrac{1}{2(V_{TH} - V_{IL})} \\ b = -\dfrac{V_{TH}}{V_{TH} - V_{IL}} \\ c = V_{DD} + \dfrac{V_{TH}^2}{2(V_{TH} - V_{IL})} \end{cases}$$

The value of d is given by $V_{DD} - V_{out}(V_{IL})$, so the estimated noise margin (11) is:

$$\hat{SNM} = V_{IL}(V_{DD}) - V_{DD} + V_{out}(V_{IL}) \tag{13}$$

Figure 4 shows the static noise margin dependence on the supply voltage for a 130nm technology inverter determined in three ways: graphically using the method of Seevinck in [2] based on the values obtained by HSPICE simulation and analytically using (10) and (13) respectively. As expected, the static noise margin is limited to $V_{DD}/2$ because of the two sides of the butterfly curve and decreases as the supply voltage is reduced from its nominal value.

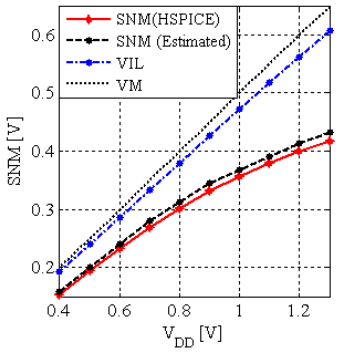

Fig. 5. SNM vs V_{DD} in 130nm technology

In figure 6 (a) and (b) is plotted the static noise margin and the relative nose margin variation on the supply voltage for 65, 90 and 130nm BPTM using (13). Figure 6 (b) illustrates the noise margin to V_{DD} ratio – the relative noise margin (rSNM = SNM/V_{DD}). This ratio increases with lowering the supply voltage up to a maximum value and than decreases. The BPTM parameters used for estimating analytically the SNM are given in [9].

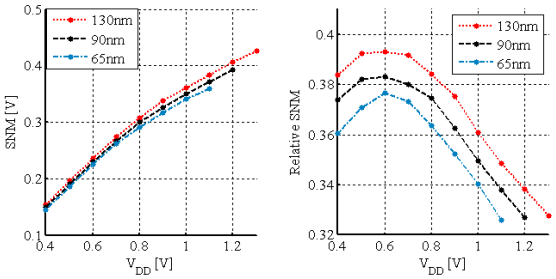

Fig. 6. (a) Estimated SNM (13) vs. V_{DD} in 130nm, 90nm, 65nm technology, (b) Relative SNM vs. V_{DD} in 130nm, 90nm, 65nm technology

Table 1 comprises the relative estimation errors for the three technologies, computed as:

$$\varepsilon V_{IL} = \frac{V_{IL} - SNM}{SNM} \cdot 100 \ [\%] \tag{14}$$

$$\varepsilon \hat{SNM} = \frac{\hat{SNM} - SNM}{SNM} \cdot 100 \ [\%] \tag{15}$$

Note that with the scaling down of the transistors, the SRAM cell's immunity to noise decreases (for a supply voltage of 1 volt, the SNM decreases with 2.8% from 130nm to 90nm and with 6% from 130nm to 65nm).

Table 1. SNM and estimation errors for 65 nm, 90 nm, 130 nm bptm in saturation region

Tech.	V_{DD}	SNM (HSP)	V_{IL} (10)	$\hat{SNM}$ (13) This work	εV_{IL} [%](14)	$\varepsilon \hat{SNM}$ [%](15) This work
130 nm	1.3	0.41	0.61	***0.43***	45.33	***3.44***
	1	0.35	0.47	***0.36***	32.39	***3.03***
	0.6	0.23	0.28	***0.24***	22.75	***2.99***
	0.4	0.15	0.19	***0.16***	24.97	***3.44***
90 nm	1.2	0.38	0.57	***0.40***	48.27	***4.92***
	1	0.34	0.47	***0.36***	38	***4.3***
	0.6	0.22	0.29	***0.23***	27.45	***4.84***
	0.4	0.15	0.19	***0.15***	30.79	***4.31***
65 nm	1.1	0.35	0.52	***0.36***	49.48	***4.42***
	1	0.33	0.48	***0.35***	43.43	***4.53***
	0.8	0.29	0.38	***0.30***	34.34	***4.41***
	0.4	0.14	0.18	***0.14***	26.52	***4.28***

2.2. Modeling SNM in Sub-threshold Region

The voltage transfer characteristic (VTC) of the CMOS in sub-threshold region has the same shape as in the above – threshold region at high supply voltages ($V_{OH} = V_{DD}$ and $V_{OL} = 0V$), but changes for low voltages ($V_{OH} < V_{DD}$ and $V_{OL} > 0V$) (figure 7).

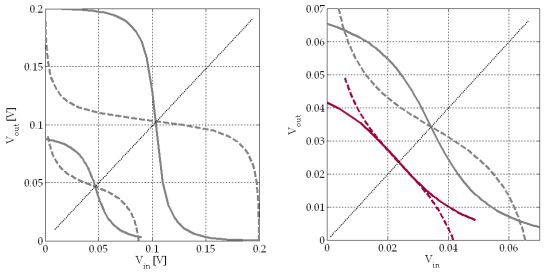

Fig. 7. VTC and $(VTC)^{-1}$ in sub-threshold region

In this situation is not enough to compute the commutation threshold voltage (V_M), it is also necessary to compute the values of the critical output voltages (V_{OH} and V_{OL}).

$$I_{D,sub-th,n} + I_{D,sub-th,p} = 0 \tag{16}$$

$$I_{D,sub-th,n} = I_{Sn} \exp\left(\frac{V_{in}}{nV_T}\right)\left(1 - \exp\left(-\frac{V_{out}}{V_T}\right)\right) \cdot \cdot \left(1 + \lambda_n V_{out}\right) \tag{17}$$

$$I_{D,sub-th,p} = I_{Sp} \exp\left(\frac{V_{in} - V_{DD}}{nV_T}\right) \cdot \cdot \left(1 - \exp\left(-\frac{V_{out} - V_{DD}}{V_T}\right)\right) \cdot \cdot \left(1 + \lambda_p \left(V_{out} - V_{DD}\right)\right) \tag{18}$$

The resulting equations were solved for:

- $V_{in} = 0$, $V_{out} = V_{OH} < V_{DD}$
- $V_{in} = V_{DD}$, $V_{out} = V_{OL} > 0$
- $V_{in} = V_{out} = V_M$

The exponential can be approximated by its Taylor series:

$$e^x = \sum_{n=0}^{\infty} \frac{1}{n!} x^n \tag{19}$$

Using this approximation, the equation (16) solved for (V_{in}, V_{out}) = (0, V_{OH}), (V_{DD}, V_{OL}) and (V_M, V_M) results in a (2n+1) order equation that can be reduced to a third order if the exponent is small.

For $V_{in} = 0$ and $V_{out} = V_{OH} < V_{DD}$ (16) becomes:

$$I_{Sn}\left(1 - \exp\left(-\frac{V_{OH}}{V_T}\right)\right)\left(1 + \lambda_n V_{OH}\right) + + I_{Sp} \exp\left(-\frac{V_{DD}}{nV_T}\right)\left(1 - \exp\left(-\frac{V_{OH} - V_{DD}}{V_T}\right)\right) \cdot \cdot \left(1 + \lambda_p \left(V_{OH} - V_{DD}\right)\right) = 0 \tag{20}$$

Using the notation $V_{OH} - V_{DD} = a$ (with $(V_{DD}-V_{OH})$ very small) together with the approximation:

$$\exp\left(\frac{a}{V_T}\right) = 1 + \frac{a}{V_T} + \frac{1}{2} \cdot \left(\frac{a}{V_T}\right)^2,$$

a third order equation in 'a' was obtained, and the values of V_{OH} are derived.

For $V_{in} = V_{DD}$ and $V_{out} = V_{OL} > 0$, (16) becomes:

$$I_{Sn} \exp\left(\frac{V_{IL}}{nV_T}\right)\left(1 - \exp\left(-\frac{V_{DD}}{V_T}\right)\right)\left(1 + \lambda_n V_{IL}\right) + I_{Sp}\left(1 - \exp\left(-\frac{V_{IL} - V_{DD}}{V_T}\right)\right) \cdot \cdot \left(1 + \lambda_p \left(V_{IL} - V_{DD}\right)\right) = 0 \tag{21}$$

With V_{IL} very small positive, the exponential can be approximated as:

$$\exp(cV_{IL}) = 1 + cV_{IL} + \frac{1}{2}(cV_{IL})^2,$$

where c is either $1/nV_T$ or $1/V_T$. So a third order equation in V_{IL} is obtained.

For $V_{in} = V_{out} = V_M \sim V_{DD}/2$, (16) becomes:

$$I_{Sn}\exp\left(\frac{V_M}{nV_T}\right)\left(1-\exp\left(-\frac{V_M}{V_T}\right)\right)(1+\lambda_n V_M) + I_{Sp}\exp\left(\frac{V_M - V_{DD}}{nV_T}\right)\left(1-\exp\left(-\frac{V_M - V_{DD}}{V_T}\right)\right)\cdot \cdot\left(1+\lambda_p(V_M - V_{DD})\right) = 0 \quad (22)$$

Using the notation $V_M - V_{DD}/2 = b$ (with $(V_M - V_{DD}/2)$ very small) and approximating the exponential as:

$$\exp(cb) = 1 + cb,$$

where c is either $1/nV_T$ or $1/V_T$. A third order equation in b is obtained, and the values of V_M are derived.

Knowing the values of the critical output voltages and the commutation threshold, the input critical voltages (V_{IL} and V_{IH}) can be estimated by using a piecewise linear approximation of the voltage transfer characteristic, as illustrated in fig. 8.

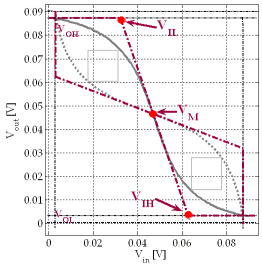

Fig. 8. Piecewise linear approximation of the VTC in sub-threshold region

The slope of the tangent to the voltage transfer characteristic in the point where $V_{in} = V_{out} = V_M$ is obtained differentiating (16) ÷ (18):

$$g = \frac{dV_{out}}{dV_{in}} = \frac{f_1(V_M)}{f_2(V_M)} \quad (23)$$

$$f_1(V_M) = -I_{Sn}\frac{1}{nV_T}\left[(1+\lambda_n V_M)\left(1-\exp\left(-\frac{V_M}{V_T}\right)\right)\right] + I_{Sp}(1+\lambda_p V_M)\left(1-\exp\left(\frac{V_M}{V_T}\right)\right)\exp\left(-\frac{V_{DD}}{nV_T}\right) \quad (24)$$

$$f_2(V_M) = I_{Sn}\frac{1}{V_T}\left[\frac{1}{V_T}(1+\lambda_n V_M) - \lambda_n\right]\exp\left(-\frac{V_M}{V_T}\right) + I_{Sn}\lambda_n + I_{Sp}\exp\left(-\frac{V_{DD}}{nV_T}\right)\left[\left(\frac{1}{V_T}(1-\lambda_p V_M) - \lambda_p\right)\cdot\exp\left(-\frac{V_M}{V_T}\right) + \lambda_p\right] \quad (25)$$

The static noise margins according to [7] are:

$$SNM_L = V_{IL} = V_M - V_{OL} + \frac{V_{OH} - V_M}{g} \quad (26)$$

$$SNM_H = V_{DD} - V_{IH} = V_{DD} - V_M - \frac{V_{OL} - V_M}{g} \quad (27)$$

Because now the characteristic in no longer symmetrical, the static noise margin will be the smaller of the two defined by (26) and (27):

$$SNM = \min(SNM_H, SNM_L) \quad (28)$$

Figure 9 (a) shows the dependence of the static noise margin on the supply voltage for a 130nm technology inverter in sub-threshold region. Comparing the two curves, a new estimation of the SNM was made.

$$\hat{SNM} = \gamma \cdot SNM \quad (29)$$

where γ is a proportionality constant obtained graphically. Figure 9(b) illustrates the SNM obtained by HSPICE simulations and the estimation given by (29).

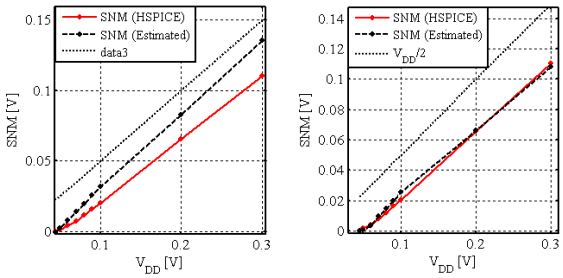

Fig. 9. (a) SNM vs V_{DD} in 130nm technology, (b) SNM vs V_{DD} in 130nm technology according to (29)

The values of the γ constant for each technology are given in Table II together with the estimation root mean square error computed as:

$$RMSE = \sqrt{\frac{\sum_{\min(V_{DD})}^{\max(V_{DD})}\left(SNM - \hat{SNM}\right)^2}{\#\ \text{samples}}} \quad (30)$$

Table 2. The values of γ and mean square error in sub – threshold region

Technology	γ	RMSE
130nm	0.8	0.0114
90nm	0.78	0.0105
65nm	0.77	0.0108

2.3. Minimum Supply Voltage for non-zero SNM

The minimum supply voltage for non-zero static noise margin is graphically determined as the value where the plot of the VTC and $(VTC)^{-1}$ looses its butterfly shape, that is where no square can be inscribed in the loops of this plot (Fig. 6). Analytically, this voltage was determined as the

value of the supply voltage where the slope to the VTC in V_M given by (23) and the slope to $(VTC)^{-1}$ in V_M computed as g^{-1} are equal to -1, or as the value of the supply voltage where the loop gain is 1. The critical values of this voltage for the three technologies are given in Table 3.

Table 3. The critical values of the supply voltage

Technology	HSPICE	Analytically
130nm	0.048 V	0.047 V
90nm	0.05 V	0.049 V
65nm	0.052 V	0.0515 V

As mentioned earlier, the SRAM cell in standby can be represented by a flip-flop consisting of two inverters as shown in figure 1(b). The gain of this loop can be determined as the product between the gains (slopes of VTC) of the two inverters, so the loop gain of the SRAM cell is given by:

$$\text{Loop Gain} = \text{gain}\left(M_{p1}, M_{n1}\right) \cdot \text{gain}\left(M_{p2}, M_{n2}\right) \quad (31)$$

Because in this paper the two inverters were considered identical the loop gain is: LoopGain = g^2, where g is given by (9) in above-threshold regime and by (23) in sub-threshold.

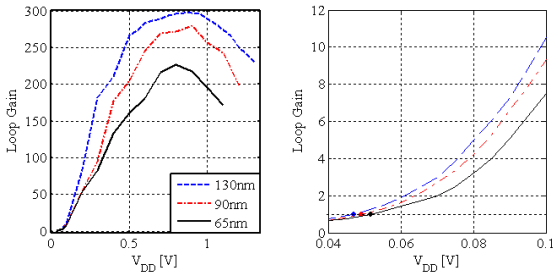

Fig. 10. (a) Loop Gain vs V_{DD}, (b) Loop Gain vs V_{DD} – the critical values of the supply voltage

The dependence of the loop gain on the supply voltage is plotted in Fig. 10(a). This has a similar behavior with the relative static noise margin, the gain increases up to a maximum and after that decreases. The critical value of the loop gain is 1. For values larger than 1 the system is bi-stable and its static noise margin is larger than 0 and for smaller values, the system looses the required bi-stability and has no noise immunity.

3. CONCLUSIONS

By lowering the supply voltage (V_{DD}) to its standby limit SRAM leakage power can be significantly reduced at the cost of reducing the robustness of the cell, expressed in terms of static noise margin (SNM). The paper investigates the effect of lowering the supply voltage from its nominal value on the robustness of a SRAM cell, by developing analytical models in above – and sub – threshold regions. The accuracy of these models was verified for 3 technologies: 130nm, 90nm and 65nm BPTM by comparing the estimated values with HSPICE simulations results. The static noise margin decreases nonlinearly with the supply voltage but the relative noise margin increases up to a maximum value and after that decreases. Because many perturbations that can affect the memory cell are related to the supply voltage this fact indicates the existence of an optimum value of the reduced supply voltage maximizing the relative SNM.

The proposed analytical model has been used to predict the minimum value of the supply voltage that preserves the data stored in the SRAM. For the BPTM analyzed these values are very small 47mV (3.7% of the nominal value) for 130 nm technology, 49mV (4.08% of the nominal value) for 90 nm technology and 51.5mV (4.68% of the nominal value) for 65 nm technology.

With scaling down of the transistors, the standard SRAM cell's immunity to noise decreases (for a supply voltage of 1volt, the SNM decreases with 2.8% from 130nm to 90 nm and with 3.2% from 90nm to 65nm technology), also at the optimum value of the supply voltage, the percentage of the supported noise decreases and the critical supply voltage increases with scale down technologies.

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