

Performance Analysis of Sliding Mode Controlled Bridgeless Interleaved Boost Converter for Battery Charging Applications

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Abstract: In the recent years, the necessity of Power Factor Correction (PFC) circuit is essential in battery charging systems, switched mode power supplies and LED (Light Emitting Diode) lighting systems. The harmonics introduced due to non-sinusoidal current drawn by the diode rectifiers can be avoided if the circuit includes active PFC circuits. In this paper, Sliding Mode Controller (SMC) design using the small signal model of Bridgeless Interleaved Boost Converter (BLIBC) for power factor correction is proposed. The control objective is threefold: (i) DC output voltage regulation under load and supply side disturbances (ii) Minimization of THD in source current ensuring improved supply side power factor (iii) Tracking of output voltage for desired reference voltage setting. The mitigation of harmonics along with regulated DC bus voltage is achieved by designing a SMC to operate at a constant switching frequency and the control law is derived following a systematic approach. The schematics are executed using MATLAB/SIMULINK[®] and the modeling is validated through the simulation results. The performance parameters are obtained for varying load and supply voltage conditions.

Keywords: Power factor Correction, Sliding Mode Control, Boost Converter, Total Harmonic Distortion, Small Signal Model, DC bus.

1. INTRODUCTION

Nonlinear loads such as Switched Mode Power Supplies (SMPS), Power Electronic Converters and Computers are the main source of harmonics which affects the Power Quality. Normally in ac to dc conversion, diode rectifiers and phase-controlled rectifiers are used. These converters draw pulsating current from the mains. This non sinusoidal current is rich in harmonics and reduces the power factor. Therefore, it is essential to implement PFC to the switch mode power supply system. A large number of authors have analyzed the effects of non-linear loads on medium and low voltage AC distribution networks and have proposed variety of methods supported by theoretical derivations and algorithms. Many of these contributions are oriented towards attempts at wave-shaping of the supply side currents close to sinusoidal variations by switching controls implemented on a compensator in the form of a power modulator (Singh et al., 2003; Madigan et al., 1999). These publications have also focused on the consequent improvement in supply side power factor (Kocher and Steigerwald, 1983; REDLT, 1994). Concurrently the question of maintaining a regulated DC voltage at the output of the non-linear rectifier/converter systems has also been addressed in many of these publications (Tse and Chow, 2000; Lu et al., 2008).

The front-end ac–dc converter is a key component of the charger system. Appropriate selection of topology plays a vital role in order to meet the necessary requirements of source current harmonics, supply side power factor and DC output voltage regulation (Agilent Technologies, 1995; IEEE,

2014; Garcia et al., 2003). The PFC is possible using basic converters such as boost converter, fly back and cuk converter etc. For regulated DC bus voltage, resonant converter involving ZVS/ZCS is also proposed to minimize the switching losses and ripple in input current (Lai et al., 2014). In the recent years, various power factor improvement techniques were addressed with modular converters, bridgeless converters and interleaved converters Nallusamy et al., 2015; Mejía-Ruiz et al., 2017). A bridgeless flyback converter with PFC is proposed for utility line system (Lin et al., 2018). The feasibility of the topology is verified by obtaining the harmonic currents from light load to heavy load under different input voltage levels. Topological modifications have also been done in bridgeless PFC converter to reduce conduction loss and current stress in semiconductors (Tseng et al., 2018). Active PFCs are widely applied to the LED lighting circuit due to the requirement of low THD and high power factor (Cheng et al., 2017).

In PFC circuits, high performance controllers are required. All these controllers include two control loops. The outer voltage mode control for DC bus voltage regulation and inner current mode control for wave shaping of input current (de Melo et al., 2010; Chattopadhyay et al., 2003). Boost converters with advanced controllers are developed for DC bus voltage regulation. Various linear and nonlinear current mode techniques are proposed and digital controllers also addressed for PFC (Umamaheswari et al., 2012; Chen and Maksimović, 2010). Linear controllers like PI Controller and Linear Quadratic Regulator (LQR) are discussed for Single Input Multiple Output (SIMO) and Multiple Input Multiple

Output (MIMO) configurations for achieving good transient and steady state responses against load and line disturbances (Augusti Lindiya et al., 2019). Among the nonlinear controllers, Sliding Mode Control (SMC) is a powerful control technique for switched mode power converters. The performance of SIMO converter with sliding mode control is analyzed (Augusti Lindiya et al., 2017) and it ensures a stable output over the range of operating loads. SMC guarantees stability for wide range of load as well as supply variation, improves transient response which makes this as an effective alternative to other conventional current mode control strategies. Despite of its advantages it suffers due to inherent drawback of variable frequency operation which is the source of electromagnetic interference. This problem can be resolved by an effective approach wherein the switching frequency of the SMC is controlled via fixed-frequency pulse-width modulation (PWM) (TAN, 2017; Yasin et al., 2018).

In this paper, an attempt is made to improve supply side power factor and output DC voltage regulation using SMC with fixed frequency PWM. Four operating modes in each half cycle are analyzed and modeling of the BLIBC is carried out with the help of equivalent circuits developed from circuit laws which ensures a relationship of physical variables in the power converter. State space equations are developed for each operating mode from which the averaged system matrix has been found.

In the proposed approach, the continuous component of control signal in SMC is derived from the equations formulated through small signal modeling of BLIBC. For successful operation of this converter, the output voltage, the inductor current and input voltage are sensed and processed. As a result, the current waveform exactly follows input sinusoidal voltage and it is also in phase with the supply voltage. The performance is analyzed by calculating THD and power factor for wide range of load variations and line voltage variations. The performance parameters obtained in this approach are better than the results available in similar publication (Gunasekaran and Vellithiruthi Thazhathu, 2017).

The rest of the paper is categorized as follows. Section 2 presents a brief review of various boost converter circuits and various modes of operation of BLIBC. In Section 3, modeling and closed loop control scheme of the converter using SMC is presented. Section 4 displays simulation studies and finally section 5 concludes the proposed work for that particular event.

2. BOOST CONVERTER CIRCUITS IN PFC AND OPERATING MODES OF BLIBC

2.1 Review of various boost converters

In most of the active PFC circuits, diode bridge rectifier is at the front end which is followed by a conventional boost converter. It provides many advantages over the other types of DC to DC converters and has excellent features like smooth input current waveform which reduces the filtering requirements hence produces less electromagnetic interference. The boost inductor is connected in series with

the source so that the inductor current is the replica of source current which makes the wave shaping easier. This topology is suitable for low and medium power applications. For high power applications, losses occur in the diode bridge increases with decrease in efficiency. Furthermore, the design of inductor for such high power levels is another problem. Hence bridgeless boost converter (Lin et al., 2018] is another alternative for high power applications. This topology reduces heat dissipation at the diode bridge rectifier, but makes the sensing circuits complex. Interleaved boost converter employs parallel combination of basic boost converters where the two switches are operated with 180° displacement. It has several advantages such as less EMI, reduced ripple in the input current, reduced conduction losses and better current sharing capability (Jang and Jovanovic, 2007). But it suffers from heat management problem at the input side similar to conventional boost topology.

The bridgeless interleaved boost converter inherently combines the advantages of both bridgeless and interleaved boost converter (Musavi et al., 2011), therefore becomes attractive now. The power circuit of BLIBC is shown in Fig. 1. The source voltage and current are represented as V_{in} and i_s . The active switch and diode in each arm is represented as Q_1, Q_2, Q_3 , and Q_4 , and D_1, D_2, D_3 , and D_4 respectively. The input side inductors of the BLIBC are represented as L_1, L_2, L_3 , and L_4 . In order to get ripple free output voltage, capacitor C is connected in parallel with the load resistor R . The output DC voltage is represented as V_o .

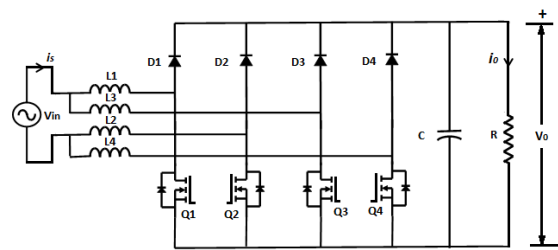


Fig. 1. Bridgeless Interleaved Boost Converter (BLIBC) Topology.

2.2 Modes of operation [Musavi et al., 2011]

The circuit operation is analyzed by considering positive and negative half cycles individually. The detailed working of BLIBC is analyzed based on the duty ratio which is less than or greater than or equal to 0.5 depending upon the range of input voltage with respect to regulated output voltage. In this paper, various operating modes of the BLIBC are explained for a duty cycle greater than 0.5. Mode 1 to Mode 4 covers the operating modes for one switching cycle during positive half of input voltage and Mode 5 to Mode 8 includes the operating modes for one switching cycle during negative half of ac input voltage

2.2.1 Mode1

During this switching interval, Q_1/Q_2 are switched ON and Q_3/Q_4 are switched OFF as in Fig. 2 (a). The current flows through L_1 and Q_1 and continues through Q_2 (and partially its body diode) and then L_2 , returning to the line. The current in these inductors increases linearly and stores energy in L_1 and

L_2 . The current in inductors L_3 and L_4 decreases linearly and energy is recovered and transferred to the load circuit through diode D_3 , C and body diode of Q_4 .

2.2.2 Mode 2

During this switching interval Q_3/Q_4 are turned ON and Q_1/Q_2 also remain in ON state as shown in Fig. 2 (b). The current in all the inductors increases linearly and stores energy. The capacitor C discharges through the load circuit.

2.2.3 Mode 3

In this mode, Q_1/Q_2 are turned off, while Q_3/Q_4 remain on, as shown in Fig. 2 (c). During this switching interval, the current in inductors L_3 and L_4 increases linearly and energy is stored in these inductors. The current flows through L_3 and Q_3 and continues through Q_4 (and partially its body diode) and then L_4 , returning to the line. The current in inductors L_1 and L_2 decreases linearly and energy is recovered and transferred to the load circuit through diode D_1 , C and body diode of Q_2 . The turning ON of Q_3/Q_4 occurs with interleaving or with a 180° phase delay.

2.2.4 Mode 4

In this mode, Q_3/Q_4 remain on, while Q_1/Q_2 are turned on, as shown in Fig. 2 (b). During this switching interval, the currents in all the inductors increase linearly and energy is stored in these inductors. The capacitor C discharges through the load circuit. This mode is similar to mode 2.

Similarly, during negative half cycle of input voltage, mode 5 to mode 8 covers four operating modes of BLIBC in one switching cycle which is shown in Fig. (d) –(f).

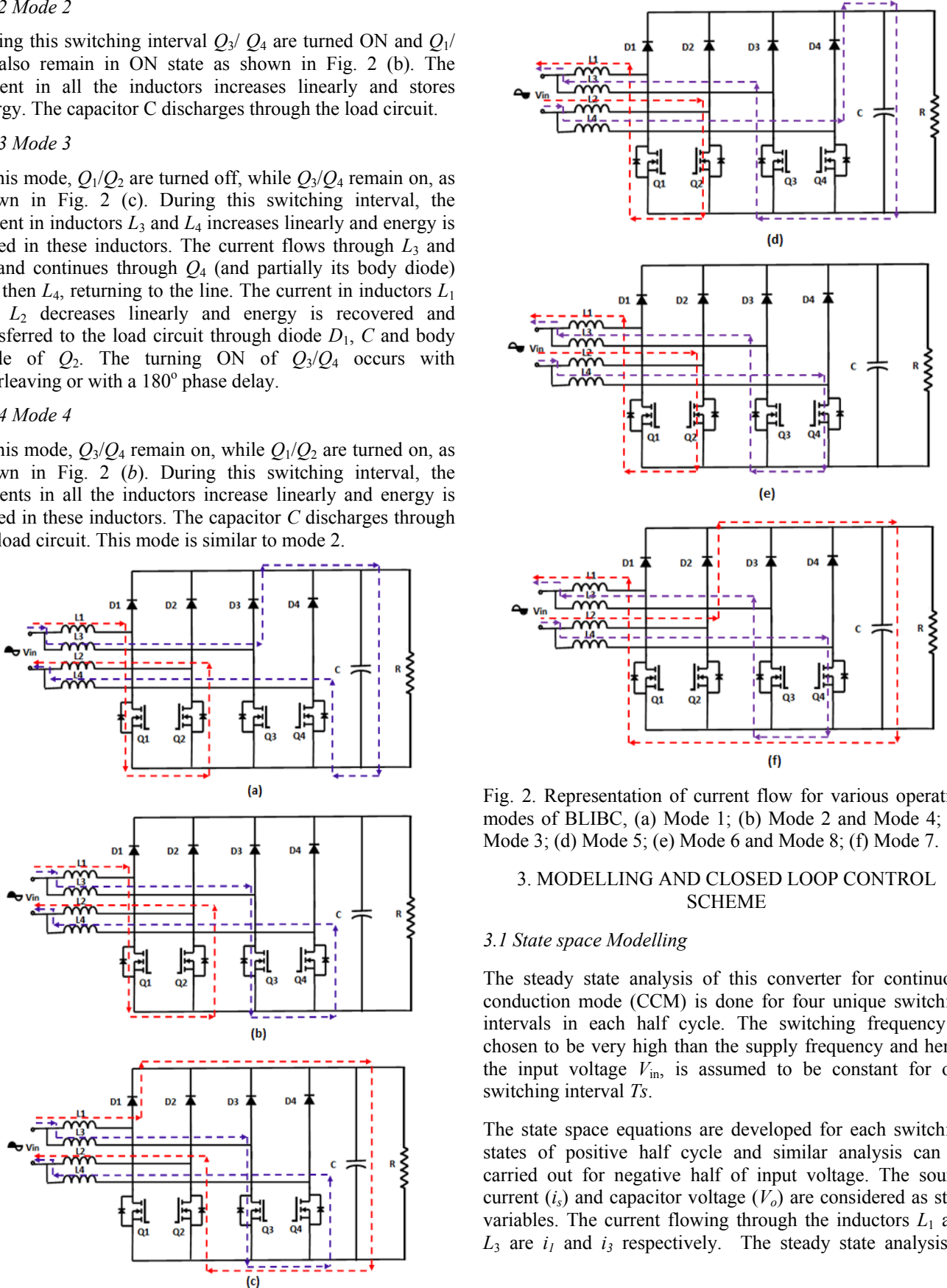


Fig. 2. Representation of current flow for various operating modes of BLIBC, (a) Mode 1; (b) Mode 2 and Mode 4; (c) Mode 3; (d) Mode 5; (e) Mode 6 and Mode 8; (f) Mode 7.

3. MODELLING AND CLOSED LOOP CONTROL SCHEME

3.1 State space Modelling

The steady state analysis of this converter for continuous conduction mode (CCM) is done for four unique switching intervals in each half cycle. The switching frequency is chosen to be very high than the supply frequency and hence the input voltage V_{in} , is assumed to be constant for one switching interval T_s .

The state space equations are developed for each switching states of positive half cycle and similar analysis can be carried out for negative half of input voltage. The source current (i_s) and capacitor voltage (V_o) are considered as state variables. The current flowing through the inductors L_1 and L_3 are i_1 and i_3 respectively. The steady state analysis is

carried out for duty cycle $D > 0.5$ and the waveforms for each sub interval are shown in Fig. 3 (Musavi et al., 2011).

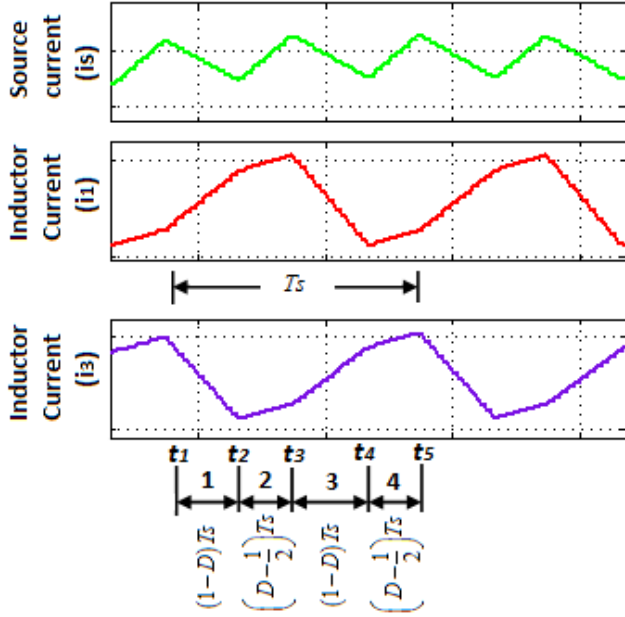


Fig. 3. Steady state waveforms for open loop control with a duty ratio $D > 0.5$.

Let the system is defined by the following state space equation

$$\dot{x} = Ax + Bu \quad (1)$$

and the output equation is represented as

$$y = Cx \quad (2)$$

where A is the system matrix of order (2×2) ; B is the disturbance matrix of order (2×1) ; C is the output matrix of order (1×2) . x is the state vector of order (2×1) , u is the disturbance vector of order (1×1) and y is the output vector of order (1×1) .

The state space equations for each operating mode are obtained using Kirchhoff's laws with reference to equivalent circuit shown in each mode. The averaged system matrix is obtained for each operating mode with a duty ratio $D > 0.5$ which are given as follows:

3.1.1 Mode 1: $(t_1 - t_2)$

Applying Kirchhoff's Voltage Law (KVL) to Fig. 4, following equations are obtained.

$$\frac{di_1}{dt} = \frac{v_{in}}{L1 + L2} = \frac{v_{in}}{2L} \quad (3)$$

Since $L1 = L2 = L3 = L4 = L$

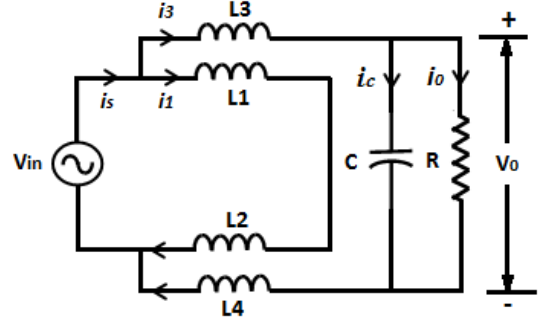


Fig. 4. Equivalent circuit during Mode 1

$$\frac{di_3}{dt} = \frac{v_{in} - v_0}{L3 + L4} = \frac{v_{in} - v_0}{2L} \quad (4)$$

$$\text{The source current } i_s = i_1 + i_3, \quad (5)$$

Differentiating (5),

$$\frac{di_s}{dt} = \frac{di_1}{dt} + \frac{di_3}{dt} = \frac{v_{in}}{L} - \frac{v_0}{2L} \quad (6)$$

Applying Kirchhoff's Current Law (KCL) to the equivalent circuit

$$i_c = C \frac{dv_0}{dt} = i_3 - i_0 = i_3 - \frac{v_0}{R} \quad (7)$$

The source current is the sum of current through the inductor L_1 and L_3 . Hence i_1 and i_3 are expressed as follows:

$$i_3 = k i_s \text{ and } i_1 = (1 - k) i_s \quad (8)$$

where k is a constant which represents fraction of total source current i_s . Hence (7) is modified as,

$$\frac{dv_0}{dt} = \frac{i_3}{C} - \frac{v_0}{RC} = \frac{k i_s}{C} - \frac{v_0}{RC} \quad (9)$$

Arranging (6) and (9) in matrix form, then state matrix and disturbance matrix for mode 1 is given as,

$$A_1 = \begin{bmatrix} 0 & -\frac{1}{2L} \\ \frac{k}{C} & -\frac{1}{RC} \end{bmatrix} \quad B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad (10)$$

3.1.2 Mode 2: $(t_2 - t_3)$

Applying KVL to Fig. 5, the following equations are obtained.

$$\frac{di_1}{dt} = \frac{v_{in}}{L1 + L2} = \frac{v_{in}}{2L} \quad (11)$$

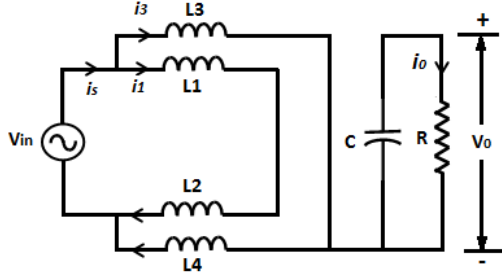


Fig. 5. Equivalent circuit during Mode 2.

$$\frac{di_3}{dt} = \frac{v_{in}}{L_3 + L_4} = \frac{v_{in}}{2L} \quad (12)$$

The source current obtained from (11) and (12) is given as,

$$\frac{di_s}{dt} = \frac{di_1}{dt} + \frac{di_3}{dt} = \frac{v_{in}}{L} \quad (13)$$

Applying KCL to Fig. 5,

$$i_c = C \frac{dv_0}{dt} = \frac{-v_0}{R} \quad (14)$$

$$\text{Hence } \frac{dv_0}{dt} = \frac{-v_0}{RC} \quad (15)$$

The state space matrix and disturbance matrix for mode 2 is obtained from (13) and (15) which are given below.

$$A_2 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{RC} \end{bmatrix} \quad B_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad (16)$$

3.1.3 Mode 3: ($t_3 - t_4$)

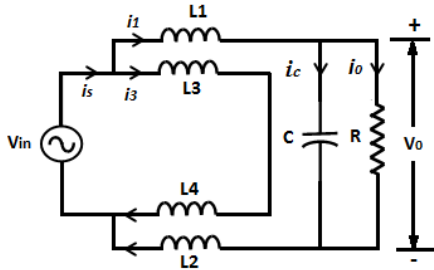


Fig. 6. Equivalent circuit during Mode 3.

Similarly, KVL is applied the equivalent circuit of BLIBC during mode 3, the following state space equations are obtained.

$$\frac{di_1}{dt} = \frac{v_{in} - v_0}{L_1 + L_2} = \frac{v_{in} - v_0}{2L} \quad (17)$$

$$\frac{di_3}{dt} = \frac{v_{in}}{L_3 + L_4} = \frac{v_{in}}{2L} \quad (18)$$

The source current is derived as follows:

$$\frac{di_s}{dt} = \frac{di_1}{dt} + \frac{di_3}{dt} = \frac{v_{in}}{L} - \frac{v_0}{2L} \quad (19)$$

Following KVL to Fig. 6, the capacitor current is expressed as,

$$i_c = C \frac{dv_0}{dt} = i_1 - i_0 = i_1 - \frac{v_0}{R} \quad (20)$$

Substituting i_1 form (8), the above equation is modified as,

$$\frac{dv_0}{dt} = \frac{i_1}{C} - \frac{v_0}{RC} = \frac{(1-k) i_s}{C} - \frac{v_0}{RC} \quad (21)$$

Arranging these (19) and (21) in matrix form and the state matrix and disturbance matrix for mode 3 are stated as follows:

$$A_3 = \begin{bmatrix} 0 & \frac{-1}{2L} \\ \frac{(1-k)}{C} & \frac{-1}{RC} \end{bmatrix} \quad B_3 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad (22)$$

3.1.4 Mode 4 : ($t_4 - t_5$)

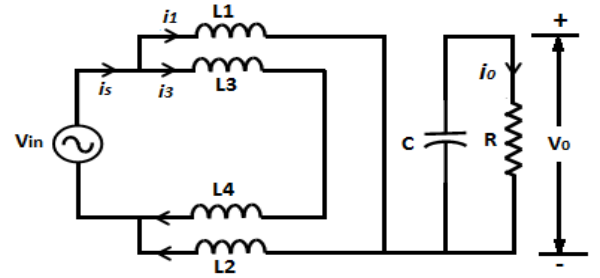


Fig. 7. Equivalent circuit during Mode 4.

The following state space equations are derived by applying Kirchhoff's laws to Fig. 7.

$$\frac{di_1}{dt} = \frac{v_{in}}{L_1 + L_2} = \frac{v_{in}}{2L} \quad (23)$$

$$\frac{di_3}{dt} = \frac{v_{in}}{L_3 + L_4} = \frac{v_{in}}{2L} \quad (24)$$

The source current is obtained from (23) and (24).

$$\frac{di_s}{dt} = \frac{di_1}{dt} + \frac{di_3}{dt} = \frac{v_{in}}{L} \quad (25)$$

Applying KCL to Fig. 7, the equation for capacitor current is obtained from which the following equation is derived.

$$\frac{dv_0}{dt} = \frac{-v_0}{RC} \quad (26)$$

Arranging (25) and (26) in matrix form, the state space matrix and disturbance matrix for mode 4 are given as follows:

$$A_4 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{RC} \end{bmatrix} \quad B_4 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad (27)$$

The state space average matrix is calculated as follows:

$$A = A_1(1-D) + A_2(D - \frac{1}{2}) + A_3(1-D) + A_4(D - \frac{1}{2}) \quad (28)$$

$$B = B_1(1-D) + B_2(D - \frac{1}{2}) + B_3(1-D) + B_4(D - \frac{1}{2}) \quad (29)$$

$$A = \begin{bmatrix} 0 & \frac{-(1-D)}{L} \\ \frac{(1-D)}{C} & \frac{-1}{RC} \end{bmatrix} \quad B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad C = [0 \quad 1] \quad (30)$$

For a duty cycle of $D < 0.5$, same state space average matrix is obtained by considering various operating modes. The BLIBC is perturbed by small variations in v_{in} causing small variations in i_s and v_o with respect to their steady state values which in turn modifies the duty ratio D . The small variations around the equilibrium point is expressed by

$$x = X + \hat{x}, \quad v_{in} = V_{in} + \hat{v}_{in}, \quad d = D + \hat{d} \quad (31)$$

The averaged small signal state space model is given as

$$\begin{aligned} \frac{d(X + \hat{x})}{dt} &= A_1((X + \hat{x})(1-D - \hat{d})) + A_2((X + \hat{x})(D + \hat{d} - \frac{1}{2})) + \\ &A_3((X + \hat{x})(1-D - \hat{d})) + A_4((X + \hat{x})(D + \hat{d} - \frac{1}{2})) + \\ &B_1((U + \hat{u})(1-D - \hat{d})) + B_2((U + \hat{u})(D + \hat{d} - \frac{1}{2})) + \\ &B_3((U + \hat{u})(1-D - \hat{d})) + B_4((U + \hat{u})(D + \hat{d} - \frac{1}{2})) \end{aligned} \quad (32)$$

The above nonlinear averaged equation is linearized about the quiescent operating point. The independent inputs of the converter are expressed as constant values i.e. DC, plus small ac variations. If the ac variations are sufficiently small in magnitude, then the nonlinear terms are much smaller than the linear ac terms, and hence can be neglected. After removing the steady state DC values, the small-signal ac model of the converter is given by

$$\begin{aligned} \frac{d\hat{x}}{dt} &= A\hat{x} + B\hat{v}_{in} + [(-A_1 - A_3 + A_2 + A_4)X + \\ &(-B_1 - B_3 + B_2 + B_4)U]\hat{d} \end{aligned} \quad (33)$$

$$\frac{d\hat{x}}{dt} = A\hat{x} + B\hat{v}_{in} + f\hat{d} \quad (34)$$

where $\hat{d}$ -small signal duty cycle and

$$f = [(-A_1 - A_3 + A_2 + A_4)X + (-B_1 - B_3 + B_2 + B_4)U] \quad (35)$$

Substituting corresponding state variables and relevant matrices A , B and f in (34) then it becomes,

$$\frac{d}{dt} \begin{bmatrix} \hat{i}_s \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1-D)}{L} \\ \frac{(1-D)}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} \hat{i}_s \\ \hat{v}_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \hat{v}_{in} + \begin{bmatrix} \frac{V_o}{L} \\ \frac{-I_s}{C} \end{bmatrix} \hat{d} \quad (36)$$

From the above equation, the control – to – output transfer function can be derived and (34) is simplified as shown below.

$$\frac{d\hat{x}}{dt} = A\hat{x} + f\hat{d} \quad (37)$$

Equation (37) is used to get the continuous component of control input u_{eq} in sliding mode control which is discussed in subsequent section.

3.2 Sliding Mode Control

The SMC, which belongs to a class of a non-linear controller offers guaranteed stability and robustness against system parameter variations, line and load uncertainties. It uses multiple state feedbacks and the desired closed-loop response is obtained in the time domain directly. All the controllable states of the system should be continuous and accessible for the SMC to be applied. In this work, a sliding mode controller is designed considering both output voltage error and input current error as state variables. The information about the voltage error is used to regulate the output voltage precisely under load disturbances whereas the inclusion of input current error information allows the source current to track closely the desired sinusoidal reference current. The control action is discontinuous as the converter is a variable structure system.

The sliding surface $\sigma(e, t)$ is chosen as a linear combination of the two state variables which is given as follows:

$$\sigma(e, t) = [G][e] = [G_1 \quad G_2] \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} \quad (38)$$

where G_1 and G_2 represents sliding coefficients, e_1 and e_2 represents error vector of the state variables (Umamaheswari, Uma and Vijayalakshmi, 2011). The discontinuous control component needed to drive the system state trajectories to the state of equilibrium can be expressed as

$$u = \text{signum}(\sigma) \quad (39)$$

The control action is capable of bringing the states of the system from any condition to the state of $\sigma = 0$. This makes the system states move towards the sliding surface and the switching function u exhibits the logic state of the switch 0 or 1. The condition for existence of sliding mode operation derived from Lyapunov's second method to determine the asymptotic stability must be satisfied in order to maintain the system states on the sliding surface. The equivalent control input u_{eq} is formulated by setting the time differentiation of (38) to zero.

Considering W as the vector containing reference of state variables, X as the actual state variable vector and e as the error vector.

4. SIMULATION RESULTS

The MATLAB[®] simulation schematic of the circuit in Fig. 1 in open loop is created and the performance of the same is evaluated by considering the specifications given in Table 1.

Table 1. Specifications of BLIBC

Parameters	Symbol	Value
Maximum value of input AC voltage	V_{sm}	18 V
Output Voltage	V_o	24 V
Duty cycle	D	0.5
Load Current	I_o	(0 - 2.5) A
Switching frequency	f_s	10 kHz
Load Resistance	R	10 Ω
Inductance	L_1, L_2, L_3 and L_4	2 mH
Output capacitance	C	6500 μ F

The MOSFET switch is triggered with a pulse obtained from a pulse generator of 10 kHz frequency. A fixed duty ratio of 50% is selected in order to get 24 V DC output from 18 V (rms) AC input. The simulation results for open loop control are shown in Fig. 9. From Fig. 9(a) it is clear that the input current is not sinusoidal for which the THD is calculated as 31.72% and the power factor is about 0.78. The DC output voltage for load current variation and source voltage variation is shown in Fig. 9(b) & 9(c). The output voltage is not regulated to 24 V for these disturbances. Hence it is essential to reduce THD and to increase the power factor by employing fixed frequency SMC.

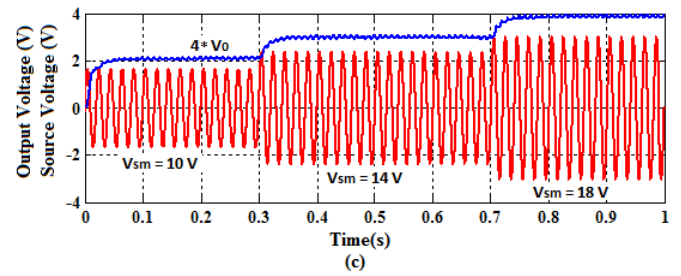
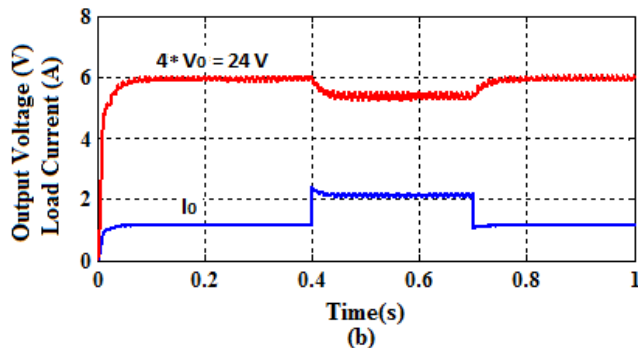
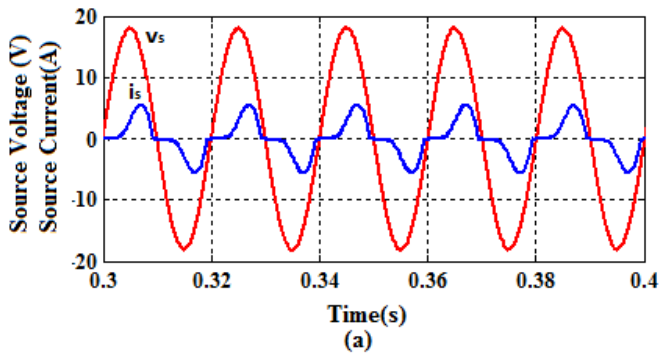
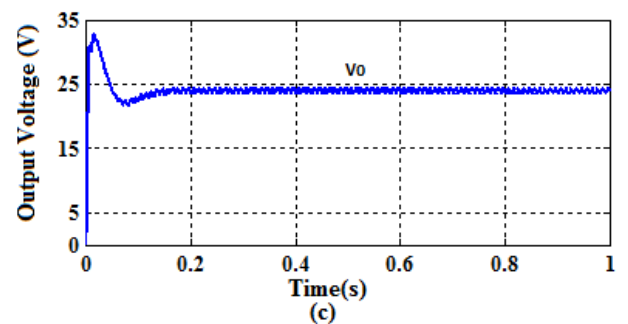
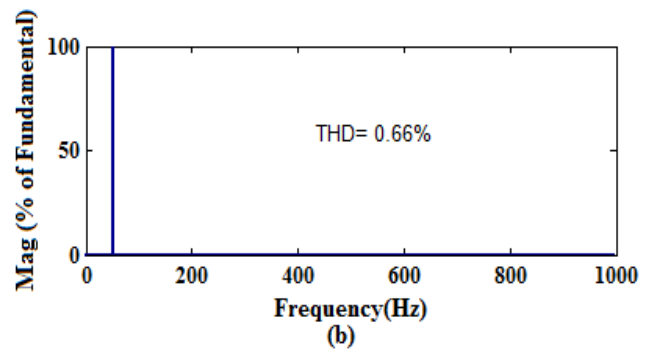
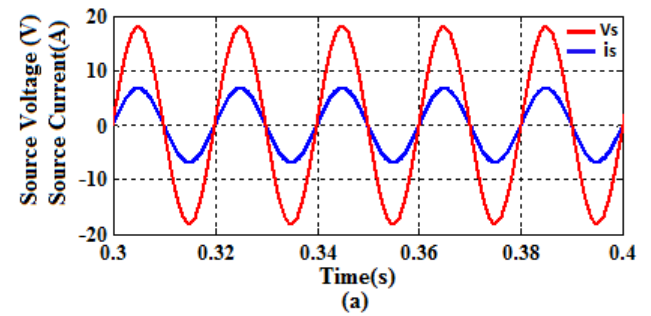


Fig. 9. Simulation waveform for open loop control, (a) Input voltage and current; (b) Load voltage and current; (c) Input voltage and output voltage.

The input current and voltage for rated loading condition are shown in Fig. 10(a). It infers that the control technique is effective to shape the input current identical to that of sinusoidal input voltage. Fig. 10(b) shows the THD of the input current which is reduced to 0.66%. The transient and steady state response of output voltage for rated load current of 2.4 A is depicted in Fig. 10(c). It shows that the required output voltage of 24 V is reached within 0.15s with an overshoot of 30%. The servo tracking of the closed loop system is verified by varying the reference voltage setting and it is seen that the output voltage exactly follows the change in V_{ref} from 24 V to 36 V and then to 48 V.



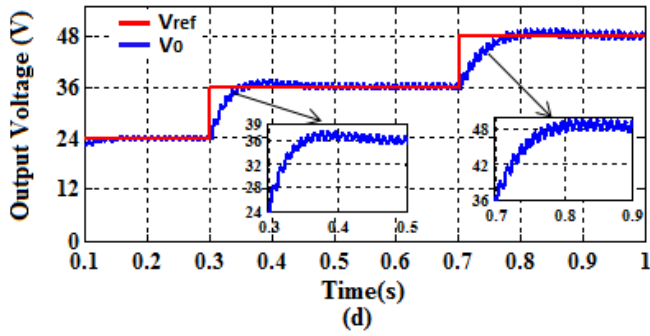


Fig. 10. Simulation waveforms, (a) Input voltage and current; (b) THD of source current; (c) Output voltage; (d) Reference voltage and actual output voltage.

Fig. 11 (a) shows the source current (i_s) and the current through the inductors L_1 and L_3 which are marked as i_l and i_3 respectively are shown in Fig. 11(b)-(c). From this source current waveform, it is seen that the ripple in the source current is reduced due to interleaving or 180° phase displacement between the inductor currents.

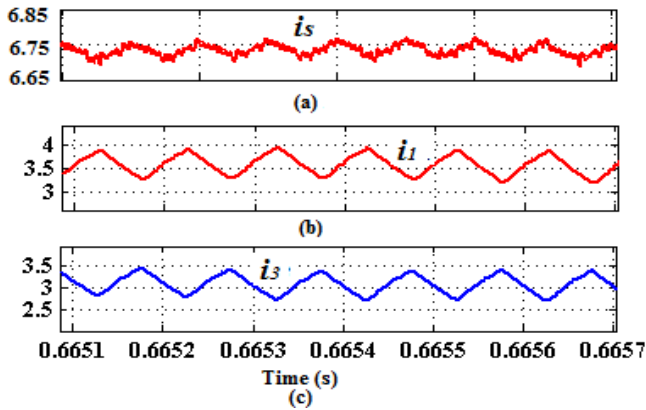


Fig. 11. (a) Source current; (b) Current through L_1 ; (c) Current through L_3 .

The amplitude of AC input voltage is varied from 10 V to 14 V and then increased to 18 V as in Fig. 12(a). It is seen from the waveform that the DC output voltage settle down to the reference voltage of 24 V within a transient interval of 120 ms for this step increase in input voltage. It is evident from Fig. 12(b) that the output voltage is well regulated for step increase in load current from 1.2 A to 2.4 A at $t = 0.4$ s and same load is maintained for a duration of 0.3 s. Then at $t = 0.7$ s, there is a step decrease in load current from 2.4 A to 1.2 A. During both the step changes, the actual load voltage gets back to V_{ref} of 24 V with a settling time of 100 ms. The source voltage and source current waveforms for this step change in load are shown in Fig. 12(c). It infers that the amplitude of the source current changes for change in load current but the controller maintains the waveshape nearly sinusoidal which improves the power factor.

The startup transient response of output voltage for varying load condition with fixed source voltage is depicted in Fig. 13(a). It concludes that the peak overshoot and settling time increases for increase in load resistance. Similarly, the

transient response of output voltage for change in input voltage with fixed load is shown in Fig. 13(b). It shows that the overshoot and settling time is reduced for decrease in input voltage.

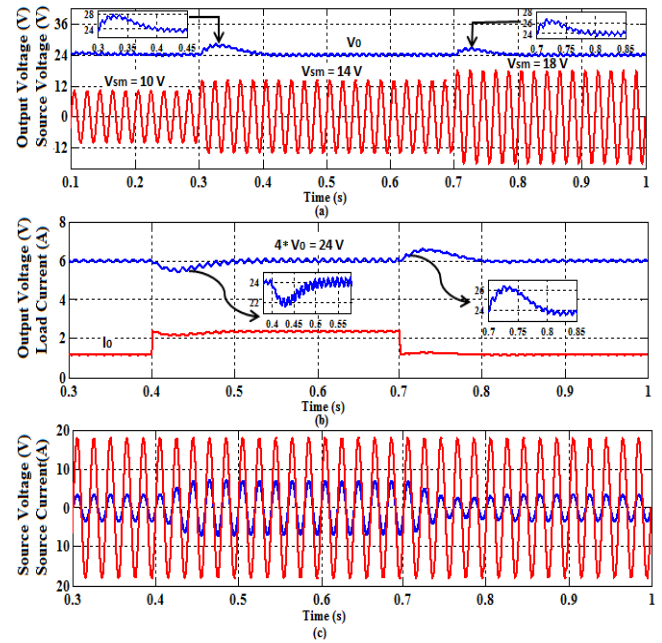


Fig. 12. Simulation waveforms, (a) Input voltage and Output voltage; (b) Output voltage and current; (c) Input voltage and current.

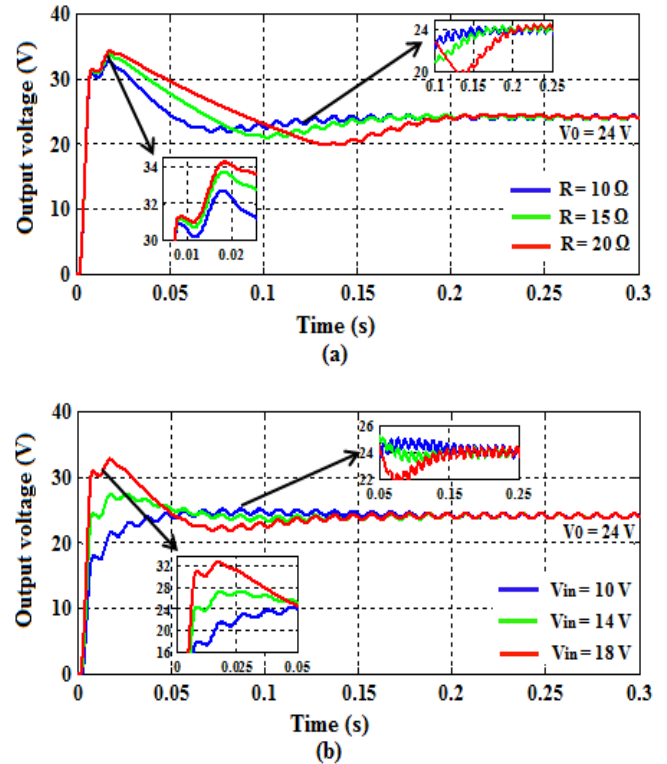


Fig. 13. (a) Transient response of output voltage for change in load resistance with $V_{in(max)} = 18$ V (b) Transient response of output voltage for change in input voltage with $R = 10\Omega$.

The performance of the converter for load variation, input voltage variation and change in reference voltage is analyzed by calculating Total Harmonic Distortion (THD) and power factor. The transient response of the converter is also analyzed by observing the overshoot (OS) and setting time (T_{ss}) under source and load side disturbances. The calculated parameters are presented in Table 2 for a reference voltage of 24 V. Similarly, the THD, T_{ss} and OS for various V_{ref} are shown in Fig. 14 (a) – (c) respectively. The THD is within the standards which shows the effectiveness of the control scheme in input current wave shaping and hence the power factor is increased above 0.99 for all the cases.

Table 2. Performance parameters for $V_{ref} = 24$ V

$V_{in} = 10$ V				
R (Ω)	THD (%)	Power Factor	OS (%)	Tss (s)
10	3.33	0.9998	2.08	0.4
12	2.55	0.9999	3.12	0.45
14	2.04	0.9999	4.58	0.52
16	1.69	0.9999	6.25	0.6
18	1.44	0.9999	7.71	0.62
20	1.25	0.9999	8.96	0.63
$V_{in} = 14$ V				
R (Ω)	THD (%)	Power Factor	OS (%)	Tss (s)
10	1.23	0.9999	5	0.3
12	0.95	0.9999	7.5	0.33
14	0.77	0.9999	9.38	0.36
16	0.67	0.9999	11.1	0.38
18	0.6	0.9999	12.5	0.39
20	0.56	0.9999	13.7	0.39
$V_{in} = 18$ V				
R (Ω)	THD (%)	Power Factor	OS (%)	Tss (s)
10	0.66	0.9999	31.2	0.15
12	0.56	0.9999	33.3	0.19
14	0.5	0.9999	35	0.2
16	0.48	0.9999	35.8	0.25
18	0.5	0.9999	36.6	0.28
20	0.52	0.9999	37.5	0.29

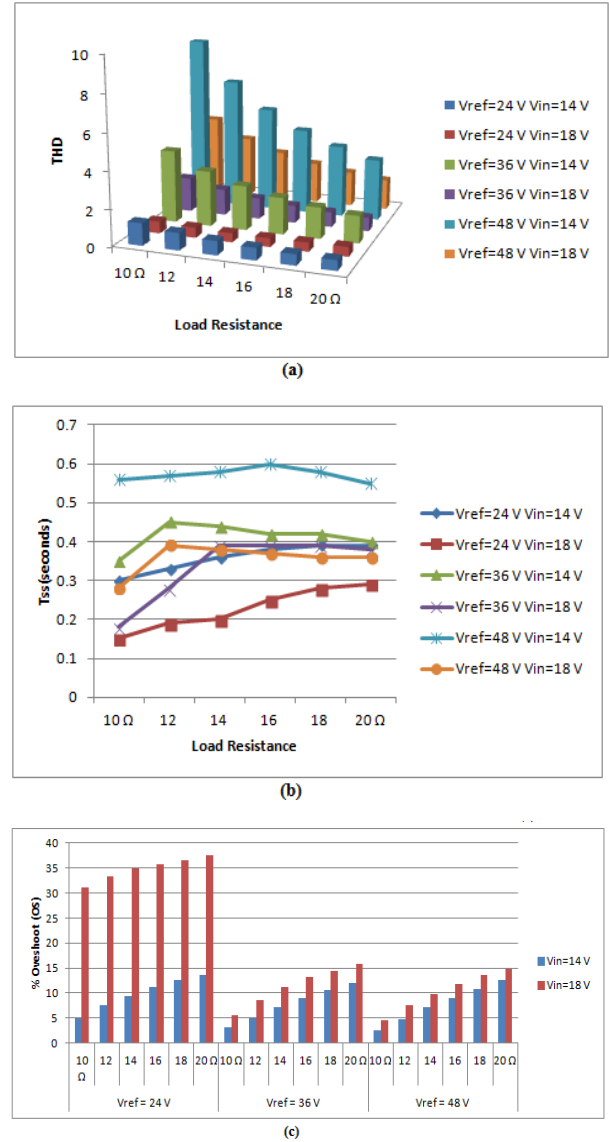


Fig. 14. (a) THD; (b) Settling Time (T_{ss}); (c) Overshoot (OS).

5. CONCLUSIONS

This work is concerned with the modeling and simulation of general purpose single phase power electronics system for delivering low voltage DC regulated output, concurrently satisfying power quality specifications viz., THD and power factor. A Bridgeless interleaved boost converter with fixed frequency sliding mode control is analyzed in this paper. Detailed state space analysis of this converter is available for various operating modes from which linearized state space matrix is obtained. In SMC, a new method of deriving the continuous component of control signal from small-signal model is proposed which provides a systematic procedure. Elaborate simulation schematic using SIMULINK[®] has been developed and the extensive simulation results have been presented for transient and steady state conditions. This control strategy which essentially generates the required reference current for supply side current shaping is governed by the respective theoretical equations and has realized highly desirable performance of the BLIBC system. The

investigation is done for evaluating the suitability and performance of the controller for wide range of input voltage and load variation. The change in reference voltage also considered for comparative evaluation. As far as the results are concerned, there is convergence of the performance as indicated by various parameters.

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