ZVS Asymmetrical PWM Full-bridge High Voltage Gain DC-DC Converter Controlled by ANFIS for Energy Harvesting Applications

A. Marikkannan*, B.V. Manikandan,**
K. Mahesh Kumar*

**Department of Electrical and Electronics Engineering, Sethu Institute of Technology, Kariapatti-626 115, Tamil Nadu, India (Tel: 091-9600235472; e-mail: mari.innofx@gmail.com, maheshkumar@sethu.ac.in)*
*** Department of Electrical and Electronics Engineering, Mepco Schlenk Engineering College, Sivakasi-626 005, Tamil Nadu, India (e-mail:bvmani@mepcoeng.ac.in)*

Abstract: Adaptive neuro-fuzzy inference system (ANFIS) controller for zero voltage switching (ZVS) asymmetrical pulse width modulated (APWM) full-bridge DC-DC converter with high voltage gain is proposed for energy harvesting applications. Converter has given continuous input current, low switching losses, higher efficiency and higher power density as a result of zero voltage switching. ANFIS controller has provided superior control to maintain constant converter output voltage for any one of energy harvesting applications. ANFIS controller performance has been compared with proportional integral (PI), fuzzy logic (FLC) and fuzzy proportional, integral and derivative (Fuzzy PID) controllers. Proposed system has been simulated using PSIM and MATLAB/Simulink tools boxes and results presented. Also, hardware prototype of proposed system with 1.6KW rating has been fabricated and tested.

Keywords: Zero Voltage Switching, DC-DC Converter, Pulse Width Modulation, High Voltage Gain, Adaptive Neuro-Fuzzy Inference System.

1. INTRODUCTION

This Present world is in the urge to discover alternate energy sources other than environmental polluting fossil fuels. Scarcity of getting fossil fuel is another one strong reason in finding alternate energy. Advent of renewable energy sources such as photovoltaic arrays, fuel cell, and wind turbine generators, turning concentration of researchers to harvest efficient energy suitable for domestic and industrial applications (Tseng et al., 2013; Ribeiro et al., 2013). Power converter especially DC-DC converter plays its major role in harvesting electrical energy from renewable energy sources with battery backup suitable for various applications and grid connected utility (Ahmed and MBleijs, 2015; Sri Revathi and Prabhakar, 2016; Chen et al., 2015; Ortega et al., 2014; Kardan et al., 2017). DC-DC converter with high voltage gain finds major applications such as electric drive, industrial lighting, battery bank charging, hybrid electric vehicles (Wen and Su 2016), and DC grid applications (Arunkumari and Indragandhi, 2017). Battery storage system is main component in delivering power to remote utility side when renewable energy sources are not available (Ribeiro et al., 2013). DC-DC converters with high voltage gain are in growing demand in high power applications such as, renewable energy sources and uninterrupted power applications (UPS). Cascading number of DC-DC step-up converter is another one method for increasing voltage gain. But overall size and components usage may large and requires complex controls. Quadratic DC-DC step up converter alleviate efficiency problem of cascade circuit and produce high quadratic voltage gain. High voltage gain and high power handling capability of converter are increased with voltage and current stresses in power switches, diodes and other magnetic elements. Hard switching and topology of converter causes these unwanted problems which reduces efficiency and power density of it (Chen et al., 2015).Various circuit topologies of high voltage gain DC-DC converter have their different requirements for particular applications (Ahmed and MBleijs, 2015). Isolated and non-isolated converter can give high voltage gain and conversion efficiency. Interleaved type high voltage gain DC-DC converter can operate wider load varying condition with wide range of zero voltage switching (ZVS) (Choi et al., 2016; Wen and Su 2016; Tohid et al., 2017). For increase power density of converter, switching frequency is increased which causes serious voltage and current stresses in power components than reduced converter size. To overcome high frequency switching problems, soft switching such as zero voltage and zero current switching in active components is traditional way in DC-DC converters. Soft switching is conventionally realized in number of ways such as by resonant tank circuit, and some additional active and passive power components. It raises power components count in addition with losses in the converter circuit and make converter bulkier with increasing of cost. Soft switching implementations also differ with topologies. In (Choi et al., 2014), a single switch DC-DC boost converter is turned on at zero current switching and turned off at zero voltage switching for wide load variations. ZVZCS is achieved in this converter using circuit formed by three diodes and two capacitors in addition with energy in leakage inductance of inductor. High voltage direct current (HVDC) transmission requires pure DC with high power high voltage gain DC-DC converter. Inductor-Capacitor (LC) parallel resonant tank circuit is used to get ZVS at turn on and off condition of switch and also gives ZCS on diodes at turned off situation

(Chen et al., 2015). Isolated high step up DC-DC converter with high efficiency is discussed (Zeng et al., 2015). Here, single switch is used and LCL resonant circuit provided ZCS during turn off condition.

Half-bridge and full-bridge DC-DC converter topologies get more attention due to its high power handling ability due to their multistage power conversion. Among them full-bridge DC-DC converter with high voltage gain leads due to its wide power utility range in high power applications. Resonant tank circuit and phase shift control are general soft switching control in full-bridge DC-DC converter (Lee et al., 2014; Lai et al., 2015). Generally, resonant tank circuit increases circuit components and phase shift control increases switching circuit more complex. To avoid this asymmetrical pulse width modulation (APWM) is implanted recently in half and full-bridge DC-DC converter to accomplish soft switching in active power components. In (Yeon et al., 2016), APWM half-bridge high voltage gain and efficiency DC-DC converter is presented and clamping technique also used to get wide ZVS range. New boost topology incorporated asymmetrical pulse width modulated (APWM) full-bridge DC-DC converter with high voltage gain is proposed. Output voltage regulation is also serious issue in high power applications.

New topology of isolated full bridge DC-DC converter as front-end converter for fuel cell is proposed (Ortega et al., 2014). Efficiency of this converter has been improved by using nanocrystalline in its passive components core. Conventional buck-boost and a boost converter combined DC-DC converter with three input port has been discussed for hybrid photovoltaic (PV)/fuel cell (FC)/battery applications (Kardan et al., 2017). It has complex structure of two unidirectional and one bidirectional input.

Voltage mode and current mode are the two modes of control strategies generally available in DC-DC converter for regulating output voltage. Classical and Optimized classical type controllers are desined for DC-DC boost converter with tedous mathematical model (Ghosh et al., 2015). Proportional and integral controller used earlier due to its robust control for industrial applications (Basaran and Sabit Cetin, 2016). But it needs tedious mathematical model calculation for non-linear characteristics of different topologies to control. Fuzzy logic controller (Bounar et al., 2014; Carvajal et al., 2000; Ismayil et al., 2010) and fuzzy proportional, integral, and derivative (PID) controller (Tang et al., 2001; Gil et al., 2015; Driss and Mansouri, 2016) are also used as a controller and they does not require mathematical model of system to control. But recent advancements in high speed microcontrollers, and digital controllers, Adaptive neuro-fuzzy inference system (ANFIS) based controller is becoming popular (Premkumar and Manikandan, 2014). ANFIS controller with combined benefits of fuzzy logic and neural network has got attention to implement as controller for asymmetrical pulse width modulation (APWM) zero voltage switching (ZVS) full-bridge DC-DC converter with high voltage gain for energy harvesting applications. Design of proposed APWM ZVS full-bridge DC-DC high voltage gain converter with fast and robust ANFIS controller makes efficient energy harvesting which is inevitable in recent power field. Simulation and real-time hardware test results are discussed to validate its merits.

2. APWM FULL-BRIDGE DC-DC CONVERTER WITH HIGH VOLTAGE GAIN

The ZVS full-bridge DC-DC converter with a high voltage gain and a very low ripple input current is shown in Fig. 1 and its theoretical waveforms of various components is shown in Fig. 2. It consists of a conventional boost converter topology with one boost inductor and an APWM full-bridge converter with a voltage doubler. The boost converter provides a very low ripple input current by utilizing boost inductors L_B, the auxiliary inductor L_{dc}, and the split dc-link capacitors C_{dc1} and C_{dc2}.

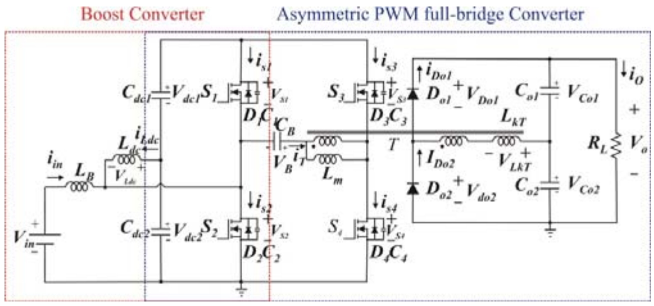

Fig. 1. ZVS APWM full-bridge DC-DC converter.

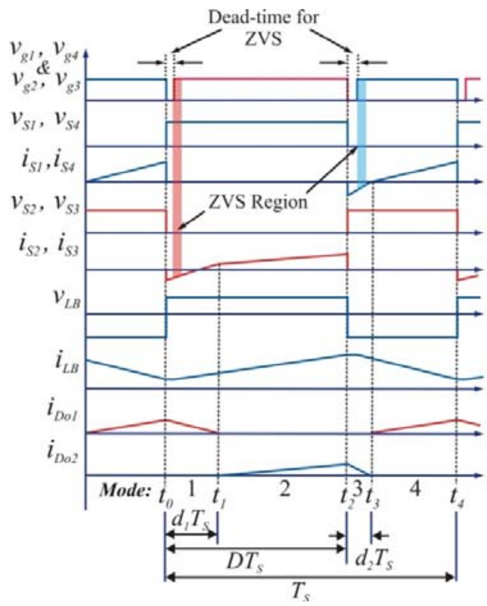

Fig. 2. Theoretical waveforms of ZVS APWM full-bridge DC-DC converter.

The APWM full-bridge converter provides a high voltage gain, a galvanic isolation, and ZVS operation to all switches S_1 through S_4. Moreover, the leakage inductance of the transformer significantly alleviates the reverse-recovery problems of the output diodes $D_{o1}$and D_{o2}. The diodes D_1 through D_4 are the intrinsic body diodes and the capacitors C_1 through C_4 are parasitic output capacitances of the full-bridge switches. The transformer is modelled as the magnetizing inductance L_m, the leakage inductance L_{kT}, and the ideal transformer which has a turn ratio of $1: n$ $(n = N_2/N_1)$. The switch S_1 & S_4 and the switch S_2 & S_3 are operated asymmetrically and the duty ratio D is based on the switch S_2 & S_3. Proposed converter comprises of four modes of operation and discussed in detail in the following section.

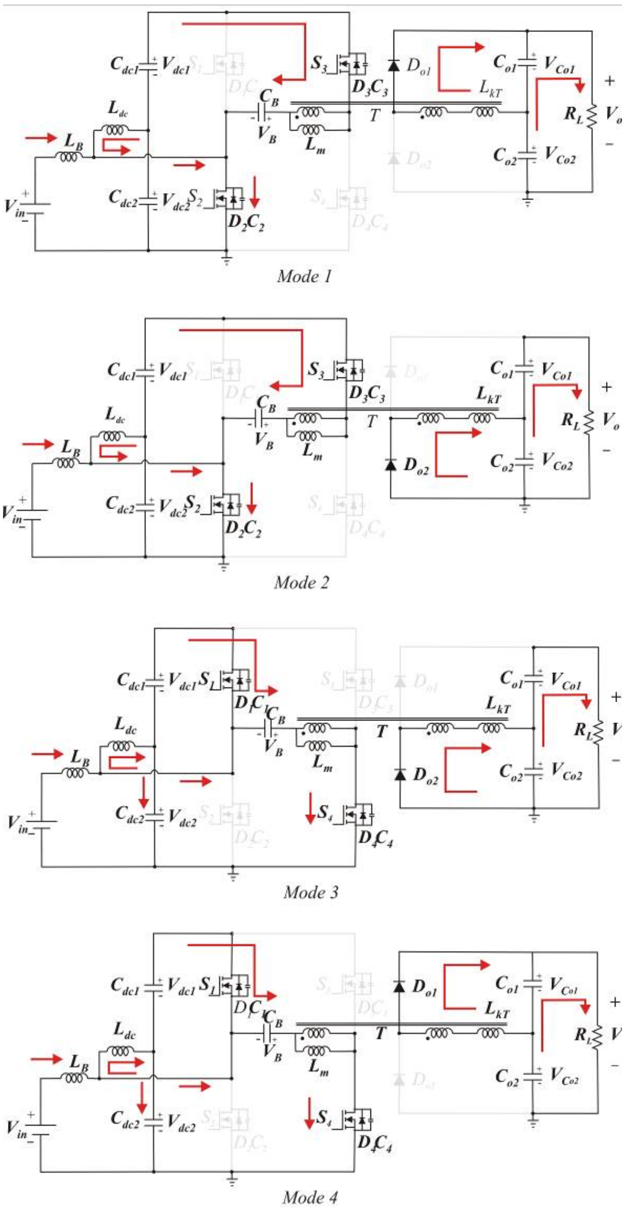

Fig. 3. Four modes of ZVS APWM full-bridge DC-DC converter.

2.1 Mode 1(t_0-t_1)

Fig. 3 represents mode 1 operation of proposed converter. Mode 1 starts with the turn-off of S_1 and S_4. But, S_2 and S_3 are yet to turn on condition and output diode, D_{o1} is turned on condition. Then, C_1 and C_4 are charged and C_2 and C_3 are discharged by using the energy stored in the magnetic components. Due to discharge of C_2 and C_3, body diodes D_2 and D_3 starts to conduct and this interval is very short due to all the parasitic output capacitances C_1 through C_4 are very small. This makes voltage across S_2 and S_3 is zero. Then, S_2 and S_3 are turned on by applying gate pulse. Now, zero voltage switching is achieved for S_2 and S_3. Inductors L_B get energy from V_{in} and L_{dc} fromV_{dc2}. Fig. 3 shows the current flow directions in various components of proposed converter in mode 1.

2.2 Mode 2(t_1-t_2)

Fig. 3 represents mode 2 operation of proposed converter. In this mode, output diode D_{o1} is turned off automatically due to secondary leakage inductor current, i_{LkT} and this current also alleviate reverse recovery problem of diode, D_{o1}. Then, diode D_{o2} starts to conduct. Except conduction of diode D_{o2}, mode 2 follows mode 1 as shown in Fig. 3.

2.3 Mode 3(t_2-t_3)

Fig. 3 represents mode 3 operation of proposed converter. Mode 3 starts with the turn-off of S_2 and S_3. But, S_1 and S_4 are yet to turn on condition and output diode, D_{o2} is turned on condition. Then, C_2 and C_3 are charged and C_1 and C_4 are discharged by using the energy stored in the magnetic components. Due to discharge of C_1 and C_4, body diodes D_1 and D_4 starts to conduct and this interval is very short due to all the parasitic output capacitances C_1 through C_4 are very small. This makes voltage across S_1 and S_4 is zero. Then, S_1 and S_4 are turned on by applying gate pulse. Now, zero voltage switching is achieved for S_1 and S_4. Then, voltage source, V_{in}, inductors L_B, and L_{dc} through C_{dc1} delivers its energy to transformer primary winding. Fig. 3 shows current flow directions in various components of proposed converter in mode 3.

2.4 Mode 4(t_3-t_4)

Fig. 3 represents mode 4 operation of proposed converter. In this mode, output diode D_{o2} is turned off automatically due to secondary leakage inductor current, i_{LkT} and this current also alleviate reverse recovery problem of diode, D_{o2}. Then, diode D_{o1} starts to conduct. Except conduction of diode D_{o1}, mode 4 follows mode 3 as shown in Fig. 3.

In the following discussion some necessary parameters used for designing the converter is given.

DC-link voltage can be calculated as,

$$V_{dc} = \frac{V_{in}}{(1-D)} \tag{1}$$

Voltages V_{dc1} and V_{dc2} between DC-link capacitors C_{dc1} and C_{dc2} are given as follows,

$$V_{dc1} = \frac{DV_{in}}{(1-D)} \tag{2}$$

$$V_{dc2} = V_{in} \tag{3}$$

Current through boost inductor L_B can be calculated from,

$$I_{LB} = \frac{V_{in}}{L_B} DT_s \tag{4}$$

Maximum inductor current I_{Ldc} is flowing through auxiliary inductor L_{dc} is given by,

$$I_{Ldc} = \frac{V_{in}}{2L_{dc}} DT_s \tag{5}$$

Voltage gain of the converter can be obtained as,

$$M = \frac{V_o}{V_{in}} = \frac{2n(1-2a)D}{(D-(2D-1)a)(1-D+(2D-1)a)} \tag{6}$$

Where,

$$d_1 = aD \tag{7}$$

$$d_2 = a(1-D) \tag{8}$$

$$a = \frac{1}{2}\left(1-\sqrt{1-\frac{4L_{kT}I_o}{nV_{in}DT_s}}\right) \tag{9}$$

Simplified voltage gain of the converter is given by,

$$M = \frac{V_o}{V_{in}} = \frac{2n}{(1-D)} \tag{10}$$

Conditions for zero voltage switching in all the switches S_1 to S_4 is, all the current through boost inductor, dc inductor and output diode must be greater than,

$$I_{zvs} = \frac{2C_{oss}V_{dc}}{T_{zvs}} \tag{11}$$

Where, C_{oss} is output capacitance of switches and T_{zvs} is transition time to achieve zero voltage switching condition.

Major drawbacks of conventional full bridge converter are high switching loss due to hard switching and exorbitant voltage stresses of switches. To reduce the voltage stresses across the switches, additional snubber circuits are required. Since, passive snubber circuits increases power loss and reduce the system efficiency, active snubber circuits are preferred for suppressing voltage stresses. However, complexity and cost of the system increases due to inclusion of extra switches. These shortcomings are easily overcome by the proposed converter without sacrificing system efficiency and performance. Moreover, in Full bridge converter, voltage doubler circuit is connected in secondary side of transformer which makes current sharing possible. Therefore, current stress and temperature will be within the limits only for proposed converter.

3. ANFIS CONTROLLER

The general ANFIS controller structure contains the same components as the FIS except for the neural network block as shown in Fig. 4. The structure of the network is composed of set of units (and connections) arranged in five connected network layers, i.e., layer1 to layer 5. The proposed ANFIS controller structure consists of four important blocks that are fuzzification, knowledge base, neural network and the Defuzzification.

Layer 1 consists of input variables (membership functions) which are error, *e* and change of error, *ce*, and Gaussian membership functions. Layer 2 is membership layer and it checks for the weights of each membership functions. It receives the input values from the first layer and act as membership functions to represent the fuzzy sets of the respective input variables. Layer 3 is called as rule layer and it receives input from the previous layer. Each node (each neuron) in this layer performs the pre-condition matching of the fuzzy rules. This layer computes the activation level of each rule and the number of layers equals the number of fuzzy rules. Each node of this layer calculates the weights which will be normalized. Layer 4 is the defuzzification layer which provides the output values resulting from the inference of rules. Layer 5 is called as the output layer which sums up all the inputs coming from layer 4 and transforms the fuzzy classification results into a crisp value (Premkumar and Manikandan, 2014).

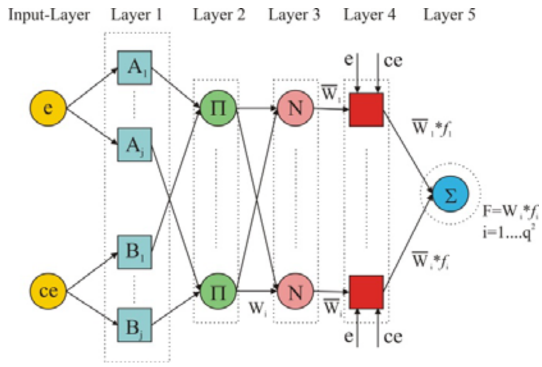

Fig. 4. Four modes of ZVS APWM full-bridge DC-DC converter.

ANFIS modelled by Takagi–Sugeno (T–S) type systems are considered and it must have the following properties: It must be first or zero order T–S type system. It should have a single output, obtained using weighted average defuzzification. All output membership functions must be of the same type and it must be either linear or constant. It must have no rule sharing, i.e., different rules cannot share the same output membership function. The number of output membership functions must be equal to the number of rules. It must have unity weight for each rule. The ANFIS structure is tuned automatically by least-square estimation and the back propagation algorithm. Because of its flexibility, the ANFIS strategy can be used for a wide range of control applications.

3.1 ANFIS controller tuning

ANFIS controller is designed in MATLAB/Simulink tool. In here data has collected for ANFIS training from fuzzy PID controller. Error, *e*, change of error, *ce*, and control output, *u* of fuzzy PID controller are collected for low range input voltage and high load condition. Collected data is used as training data of ANFIS as shown in Fig. 5. ANFIS training error plot is shown in Fig. 6.

From the plot of training error, it is clear that the fuzzy inference system has been fine trained with minimum error of 0.0133. The testing of trained data with testing data is shown in Fig.7. It has provided a clear view of the fact that, ANFIS output closely matches to the actual control output of ANFIS even at training error of 0.0133.

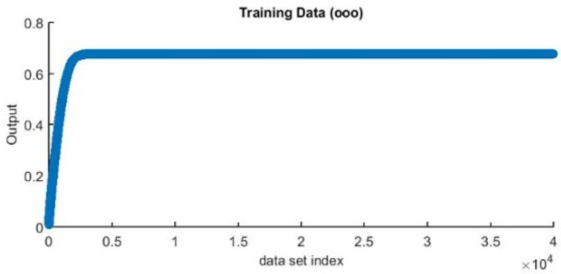

Fig. 5. ANFIS Training data plot.

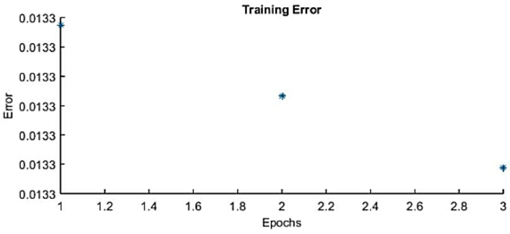

Fig. 6. ANFIS Training error plot.

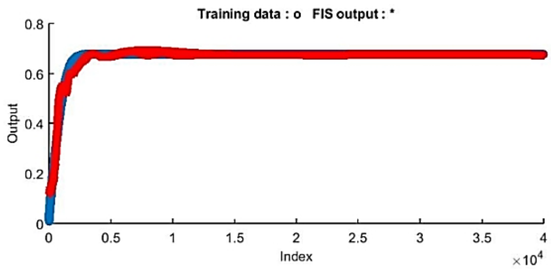

Fig. 7. Testing of ANFIS trained data with rest data.

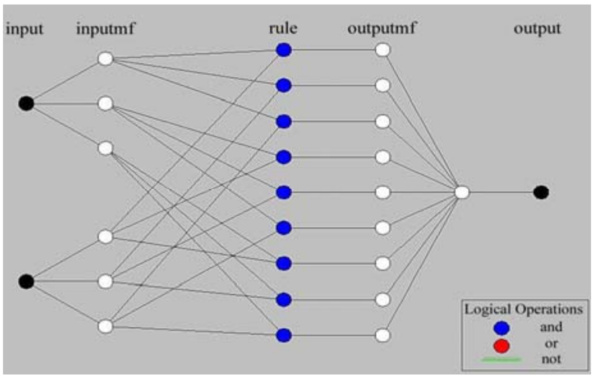

Fig. 8. ANFIS controller structure.

The proposed ANFIS structure generated by Matlab/Simulink tool box is shown in Fig. 8. It consists of five layer network and first layer is the input layer (error, e and change of error, *ce*). The input membership function layer is the next layer and inputs are distributed with three fuzzy sets. In the third layer the inputs and outputs are linked with AND operator. The output membership function layer has been distributed with nine constant values in the fourth layer. Output layer is the last layer which sums up all the inputs coming from the previous layer and transforms the fuzzy classification results into a crisp value.

The membership functions for each input, which are learned by ANFIS are shown in Fig. 9(a) & (b). Nine fuzzy rules are derived from six input membership functions. Gaussian membership functions are used in this proposed ANFIS reference model. According to the input and output membership mapping, these rules are derived, so as to produce control signal for error, *e* and change of error, *ce*.

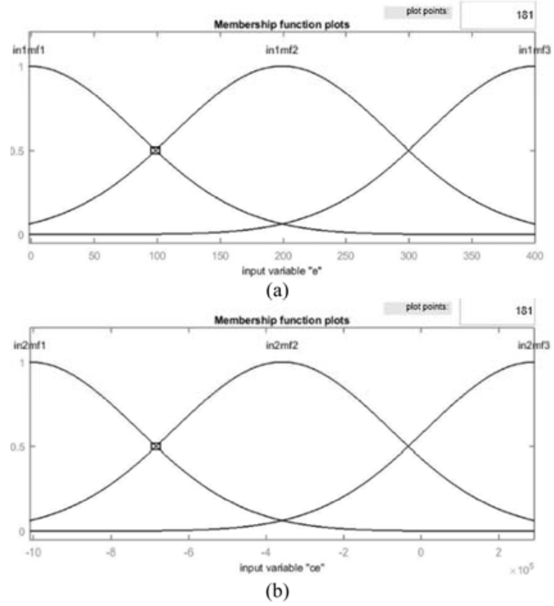

Fig. 9. Membership function of ANFIS inputs after learning (a) Membership function for error, *e* (b) Membership function for change of error, *ce.*

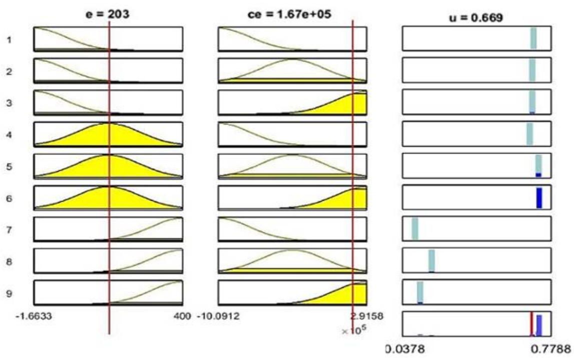

Fig. 10. Rule view of T-S FIS of ANFIS controller.

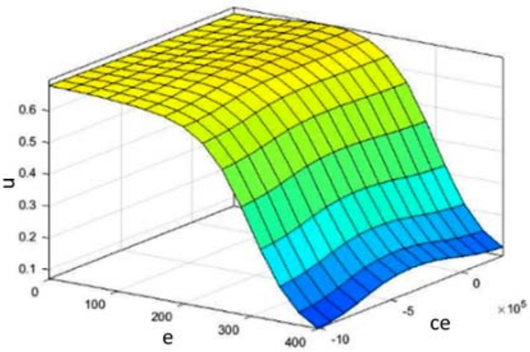

Fig. 11. Surface view of T-S FIS of ANFIS controller.

After the training, final rule base for fuzzy inference system is generated and shown in Fig. 10 and Fig. 11 shows the fuzzy rule base which is generated as surface view. This 3-dimensional plot is drawn between the parameters of error, *e*, change of error, *ce*, and control output, *u*.

4. SIMULATION RESULTS AND DISCUSSION

ANFIS controlled APWM full-bridge DC-DC converter with high voltage gain is simulated in MATLAB/Simulink and PSIM/Simcoupler as shown in Fig.12 & 13 respectively. Converter is simulated using platform of PSIM software and ANFIS controller using MATLAB/Simulink. Both these platform is bridged using PSIM/Simcoupler tool which is dedicated for integration of PSIM with MATLAB. Table 1 shows the circuit parameters of the converter.

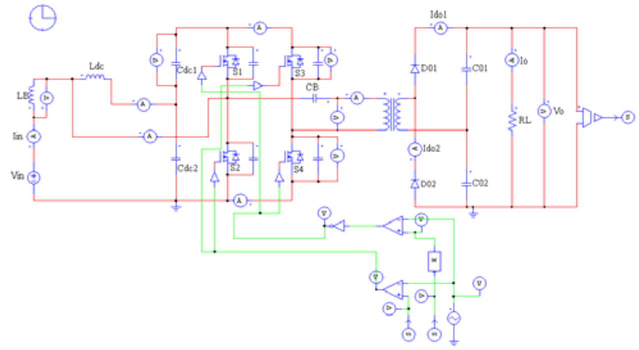

Fig. 12. PSIM simulation circuit of ZVS APWM full-bridge converter.

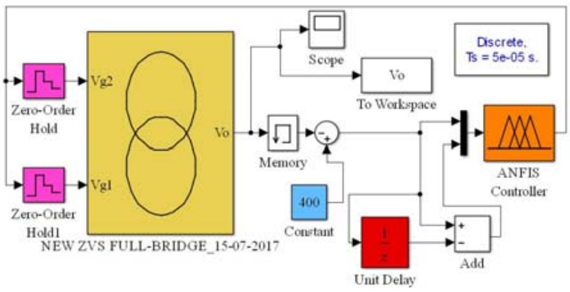

Fig. 13. Matlab/Simulink model of ANFIS controller for converter.

Table 1. Circuit parameters of converter for simulation

Parameter	Value
Inductance L_B	800µH
Inductance L_{dc}	33 µH
Output capacitance, C_o	470µF
DC-blocking capacitor, C_B	6.6 µF
DC link capacitance C_{dc1} and C_{dc2}	470µF
Transformer turns ratio, n	1:3
Primary magnetizing inductance L_m	150 µH
Secondary leakage inductance L_{ks}	7µH

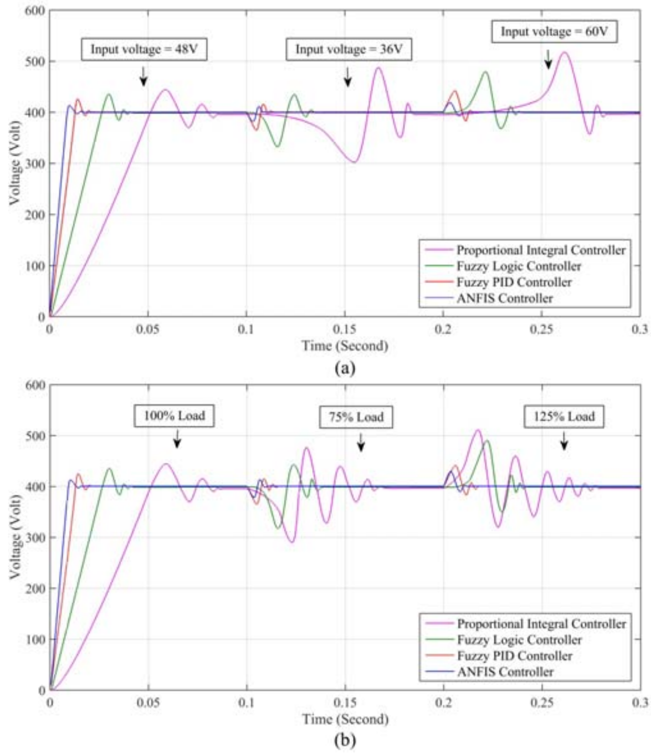

Fig. 14. Simulation responses of converter for (a) Line regulation (b) Load regulation.

Simulation output is obtained for change in input voltage of converter and connected load. A resistive load is used for variable load imitation. Fig.14(a) shows the simulation responses for dynamic changes in input voltage of full-bridge DC-DC converter from 48V (rated input) to 24V (50% of input voltage) and then to 72V (150% of input voltage). Connected load varies from 100% to 50% and then to 150% and converters simulated responses are plotted as shown in Fig.14(b). Proportional integral (PI) controller takes long time to settle with large oscillations. This is unwanted situation for energy harvesting or any application. Fuzzy logic controller shows improved response than PI controller. But it also takes some long time with little oscillations to stable. Nearest expected responses are shown in fuzzy PID controller performances with high overshoot. ANFIS controller gives fast responses with low overshoot which is acceptable in energy harvesting applications. Observed performance parameters are displayed in Table. 2.

Table 2. Performance parameters for various controllers in simulation.

Controller	Rise time in second	Settling time in second	Overshoot In volt	Steady-state error in volt	Output Voltage in volt
PI controller	0.0512	0.0343	44.6	4.2	395.8
Fuzzy Logic Controller	0.0267	0.0158	35.4	1.4	398.6
Fuzzy PID controller	0.0129	0.0088	26.5	-0.5	400.5
ANFIS controller	0.0089	0.0083	12.6	0.4	400.4

5. EXPERIMENTAL RESULTS AND DISCUSSIONS

Experimental setup of proposed ANFIS controlled ZVS APWM full-bridge DC-DC converter with high voltage gain for 1.6KW power rating is shown in Fig.15. ARDUINO Mega 2560 is used for ANFIS controller and 2.5KW resistive load is used as load for the converter. Table 3 shows the list of various components and its values used for experimental setup of the converter for real-time validation of simulated results.

Both line regulation and load regulation is done to validate the simulation results in real-time. Fig. 16(a) & (b) shows experimental results of output voltage and current which are captured for line voltage regulation from 48V to 60V and 48V to 36V respectively. Experimental results of voltage and current waveforms for load variations are displayed in Fig. 16(c) & (d). Load is varied from 100% to 125% and then from 100% to 75% as shown. It is observed that, experimental results have given same response as simulation response with small variation due to practical design. Based on experimental results, ANFIS controller has given fast and stable responses for both line and load regulations. Observed performance parameters for experimental results are shown in Table 4.

Table 3. Components values used for the experimental set up.

Parameter	Value
Input voltage, V_{in}	36-60V
Switching frequency, f_{SW}	100KHz
Output voltage, V_o	400V
MOSFET(S_1,S_2,S_3 & S_4)	IXFH22N60P3
Output Diode (Ultra-fast recovery diode)	RURG3060
Primary magnetizing inductance L_m	153.4μH
Secondary leakage inductance L_{ks}	9.3μH

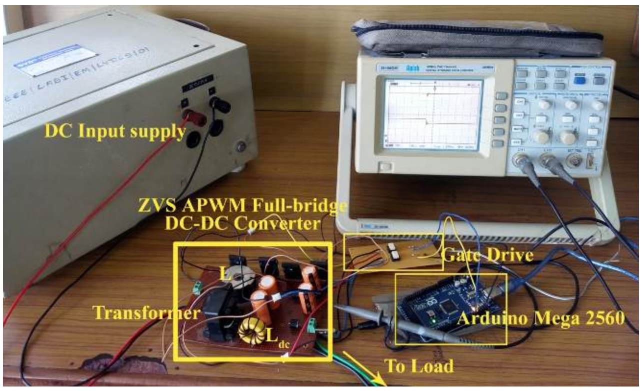

Fig. 15. Experimental hardware setup of ZVS APWM full-bridge DC-DC converter.

APWM full-bridge DC-DC converter has provided very high efficiencies in soft switching condition as compared to hard switching and it is clearly displayed in Fig.17. Zero voltage switching in this converter has considerably improved the efficiency and thereby it has proven its worthiness for energy harvesting as well as various applications.

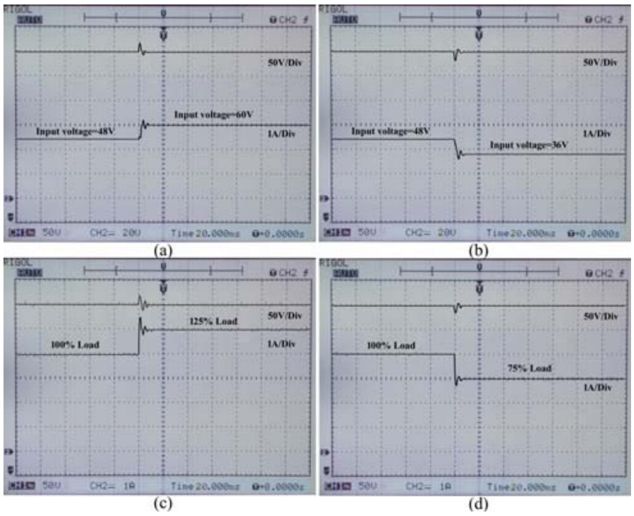

Fig. 16. Experimental output voltage and current waveforms for (a) & (b) line regulation and (c) & (d) load regulation

Table 4. Performance parameters from experimental output.

	Settling time (seconds)	Steady-state error (volt)
ANFIS controller (line volt regulation)	0.00932	2V
ANFIS controller (load regulation)	0.00927	2.5V

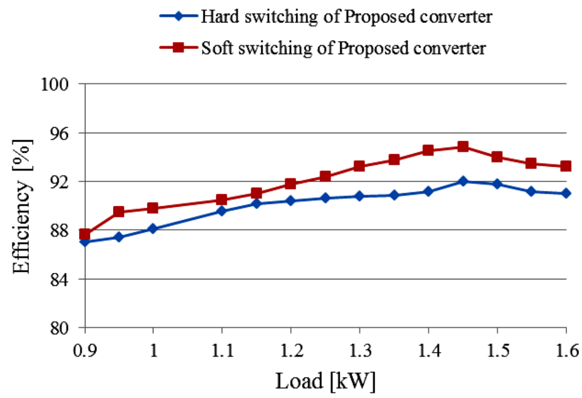

Fig. 17. Experimental measured efficiency of ZVS APWM full-bridge DC-DC converter.

6. CONCLUSION

ANFIS controlled APWM full-bridge DC-DC converter with high voltage gain for energy harvesting applications has been proposed. Proposed controller makes the converter to provide continuous and low ripple input current and low ripple regulated output voltage. APWM technique gives soft zero voltage switching (ZVS) across active power switches and zero current switching (ZCS) in diodes connected in transformer secondary side. ANFIS controller performance has been evaluated with proportional integral, fuzzy logic, and fuzzy PID controller. ANFIS controller gives good and fast dynamic response to stabilize output voltage of converter compared with other three controllers. Finally, proposed system has been realised in experimental hardware setup for power rating of 1.6KW. Both simulation and experimental responses has given almost same replica of results.

REFERENCES

Ahmed, O.A. and MBleijs, J.A. (2015), An overview of DC–DC converter topologies for fuel cell-ultracapacitor hybrid distribution system. *Renewable and Sustainable Energy Reviews,* vol. 42, pp. 609-626.

Arunkumari, T. and Indragandhi, V. (2017), An overview of high voltage conversion ratio DC-DC converter configurations used in DC micro-grid architectures. *Renewable and Sustainable Energy Reviews*, 77, 670-687.

Basaran, K. and Sabit Cetin, N. (2016), Designing of a fuzzy controller for grid connected photovoltaic system's converter and comparing with PI controller. *IEEE International Conference on Renewable Energy Research and Applications (ICRERA)*, Birmingham, UK, (pp. 102–106). IEEE.

Bounar, N., Boulkroune, A., and Boudjema, F. (2014), Adaptive Fuzzy Control of Doubly-Fed Induction Machine. *Journal of Control Engineering and Applied Informatics,* 16(2), 92-110.

Carvajal, J, Chen, G. and Ogmen, H. (2000), Fuzzy PID controller: Design, performance evaluation, and stability analysis. *Elsevier journal on Information Sciences,* vol. 123, no. 3–4, pp. 249-270.

Chen, W., Wu, X., Yao, L., Jiang, W. and Hu, R.(2015), A Step-up Resonant Converter for Grid-Connected Renewable Energy Sources. *IEEE Transaction on Power Electronics,* 30(6), 3017 – 3029.

Chen, Z, Zhou, Q. and Xu, J. (2015), Coupled-inductor boost integrated flyback converter with high-voltage gain and ripple-free input current. *IET Power Electronics,* 8(2), 213-220.

Choi, B.H, Lee, S.W., Thai, V.X. and Rim, C.T. (2014), A Novel Single-SiC-Switch-Based ZVZCS Tapped Boost Converter. *IEEE Transaction on Power Electronics,*29(10), 5181 – 5194.

Choi, H., Jang, M., Ciobotaru, M. and Agelidis, V.G. (2016), Performance evaluation of interleaved high-gain converter configurations. *IET Power Electronics,* 9(9), 1852 – 1861.

Driss, Z. and Mansouri, N. (2016), A novel adaptive approach for synchronization of uncertain chaotic systems using fuzzy PI controller and active control method. *Journal of Control Engineering and Applied Informatics,* 18(3), 3-13.

Gil, P., Lucena, C, Cardoso, A. and Palma, L.B. (2015), Gain Tuning of Fuzzy PID Controllers for MIMO Systems: A Performance-Driven Approach. *IEEE Transaction on Fuzzy Systems*, 23(4), 757 – 768.

Ghosh, A. and Banerjee, S. (2015), Control of Switched-Mode Boost Converter by Using Classical and Optimized Type Controllers. *Journal of Control Engineering and Applied Informatics,*17(4), 114-125.

Ismail, N.F.N, Musirin, I., Baharom, R. and Johari, D. (2010), Fuzzy logic controller on DC/DC boost converter. Power and Energy (PECon), 2010 IEEE International Conference on, 29 Nov.-1 Dec. 2010.

Kardan, F., Alizadeh, R. and Reza Banaei, M. (2017), A New Three Input DC/DC Converter for Hybrid PV/FC/Battery Applications. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 5(4), 1771 – 1778.

Lai, Y.S., Su, Z.J. and Chang, Y.T. (2015), Novel Phase-Shift Control Technique for Full-Bridge Converter to Reduce Thermal Imbalance Under Light-Load Condition. *IEEE Transaction on Industry Applications*, 51(2), 1651-1659.

Lee, Y.C., Kim, H.K., Kim, J.H. and Hong, S.S. (2014), A Study on Implementing a Phase-Shift Full-Bridge Converter Employing an Asynchronous Active Clamp Circuit. *Journal of Power Electronics*, 14(3), 413–420.

Nouri, T., Vosoughi, N., Hosseini, S.H. and Sabahi, M. (2017), A Novel Interleaved Nonisolated Ultrahigh-Step-Up DC–DC Converter With ZVS Performance. *IEEE Transaction on Industrial Electronics*, 64(5), 3650 – 3661.

Ortega, M., Jurado, F. and Valverde, M. (2014), Novel topology for DC/DC unidirectional converter for fuel cell. *IET Power Electronics,* 7(3), 681 – 691.

Premkumar, K. and Manikandan, B.V. (2014), Adaptive Neuro-Fuzzy Inference System based speed controller for brushless DC motor. *Journal of Neurocomputing,* 138, 260–270.

Ribeiro, E., Cardoso, A.J.M. and Boccaletti, C. (2013), Fault-tolerant strategy for a photovoltaic dc-dc converter. *IEEE Transaction on Power Electronics,* 28(6), 3008-3018.

Sri Revathi, B. and Prabhakar, M. (2016), Non isolated high gain DC-DC converter topologies for PV applications – A comprehensive review. *Renewable and Sustainable Energy Reviews*, 66, 920-933.

Tang, K.S., Man, K.F., Chen, G. and Kwong, Y. (2001), An optimal fuzzy PID controller. *IEEE Transaction on Industrial Electronics,* 48(4), 757 – 765.

Tseng, K.C., Huang, C.C., and Shih, W.Y. (2013), A high step-up converter with a voltage multiplier module for a photovoltaic system. *IEEE Transaction on Power Electronics,* 28(6), 3047-3057.

Wen, H. and Su, B. (2016), Hybrid-mode interleaved boost converter design for fuel cell electric vehicles. *Energy Conversion and Management,* 122, 477-487.

Yeon, C.O., Lee, J.B., Lee, I.O., and Moon, G.W. (2016), Wide ZVS Range Asymmetric Half-Bridge Converter With Clamp Switch and Diode for High Conversion Efficiency. *IEEE Transaction on Industrial Electronics,* 63(5), 2862 – 2870.

Zeng, J., Qiao, W. and Qu, L. (2015), LCL-resonant single-switch isolated DC–DC converter. *IET Power Electronics,* 8(7), 1209 – 1216.