Modified Single-Phase Adaptive Transfer Delay Based Phase-Locked Loop with DC Offset Compensation

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Abstract: The phase-locked loops (PLL) represent a major component in different types of grid-connected power conversion applications. The main function of the single-phase PLLs represents the input quadrature signal generation (QSG), which can be performed by various algorithms. In this paper, the modified adaptive transfer delay single-phase PLL (ATD-PLL), which includes the input signal DC offset compensation, is used for the synchronization with the single-phase input signal, and for the positive sequence component separation and synchronization in a case of a three-phase application. The small-signal ATD-PLL dynamic analysis is performed, accompanied by a corresponding PLL parameter tuning procedure. The novel ATD-PLL performance is verified by simulation and experimental tests, proving its effectiveness, accuracy, and improved dynamic performance.

Keywords: Frequency and phase estimation, phase-locked loop, transfer delay, quadrature signal generation, dc offset compensation

1. INTRODUCTION

In the single-phase PLL applications the QSG can be performed by means of a wide range of different algorithms (Han et. al., 2016), resulting in various types of single-phase PLL applications (Golestan et. al., 2017a). In this paper, a modified transfer delay (TD) (3 Golestan et. al., 2016) based QSG is analyzed and considered for application. Namely, the main advantage of TD-PLL resides in its simplicity of implementation, which is accompanied by typical problems related to the double nominal frequency component in the estimated frequency caused by the input signal frequency variation from the nominal value, and to the characteristic estimated phase angle offset (Golestan et. al., 2017b).

However, the QSG can, also, be addressed by different other means. Apart from the TD-PLL, which represents one of the earliest forms of QSG, the derivative based (DER) (Guan et. al. 2017) solution can, also, be used as one of the simpler approaches. Nevertheless, the DER based algorithms are rarely used, due to their increased sensitivity in relation to the measurement noise an to the grid voltage distortions.

In order to enable more robust PLL performance and a higher level of grid voltage disturbance rejection, adaptive filter (AF) based QSG solutions are proposed. One of the main AF based solutions is represented by the second-order generalized (SOGI) (Ciobotaru et. al., 2006) based QSG, which enables a significant level of filtration and variable nominal frequency operation. In order to improve the grid voltage disturbances filtration, the multiple SOGI solution is proposed (Rodriguez et al. 2011), consisting of a series of SOGI blocks. In (Karimi-Ghartemani et. al. 2012) an integrator is added to a conventional SOGI in order to enable the rejection of the DC offset present at the input signal. Finally, the equivalent dynamic performance and disturbance filtering to SOGI can be achieved by means of inverse-Park based (PARK) (Wang et. al. 2012), which is analytically proven in (Golestan et. al., 2013).

Furthermore, in order to overcome the dynamic limitations introduced in SOGI by the nonlinear adaptive filtering operation, the frequency-fixed PLL is proposed based on a SOGI with fixed nominal frequency (Xiao et. al., 2017), showing that a significant improvement in the PLL dynamic performance can be achieved by these means.

Regarding the TD based QSG realizations, which represent the main subject of the paper, they can be classified into two main groups: (i) fixed and (ii) variable transport delay. In (Dai et al., 2018), the fixed TD based frequency estimation scheme is proposed, based on a linear regression grid voltage model. In this way, a robust estimator operation is achieved, immune in relation to the grid voltage disturbances. In (Dai et. al. 2019), a linear regression grid voltage model is, also, employed, which includes both frequency and phase angle estimation. In this way, stable PLL and operation is achieved, which is immune in relation to the input signals DC offset. In (Golestan et. al., 2017c), fixed TD based PLL technique is proposed based on a least-error squares method, used for a grid voltage frequency and phase angle estimation, and, also, for harmonic, positive and negative sequence components decomposition. In (Yang et. al., 2016), in order to solve the problem related to the fixed TD and variable input signal frequency, a virtual-unit delay based PLL is proposed, based on the time delay approximation by means of a linear interpolation polynomial. Consequently, in (Golestan et.

al., 2019) a conventional three-phase based delayed signal cancellation technique is adopted for a single-phase realization.

In (Batista et. al., 2015), variable structure delayed signal cancellation based algorithm is proposed, with the varying structure employed in order to improve the PLL dynamic performance for different harmonic input signal contents. Finally, in (Golestan et. al., 2018) comprehensive analysis of the variable-length TD based QSG techniques is presented, including the small-signal modeling and the resulting PLL parameter tuning procedure.

Regarding the single-phase PLL DC offset compensation, there are SOGI (Karimi-Ghartemani et. al. 2012) and observer (Park et. al., 2017) based solutions. Furthermore, in (Zheng et. al., 2016) weighted least squares estimation (WLSE) based solution is proposed that enables PLL operation with improved dynamic performance with increased algorithm complexity. In (Golestan et. al., 2015), a comprehensive survey of PLL algorithms with input DC offset compensation is presented.

In this paper, a modified and version of single-phase ATD-PLL (Golestan et. al., 2017b) is presented. Namely, for the first time, the ATD based PLL is proposed that is immune in relation to the input signal DC offset, with the improved dynamic response when compared to similar existing solutions. Furthermore, for three-phase systems, the novel ATD based PLL is proposed for the positive and negative sequence components separation in the input signals. Consequently, the proposed solution is compared with a reference observer based proposed in (Karimi-Ghartemani et. al. 2012) that is, also, immune in relation to the input signal DC bias.

This paper consists of six sections. In Section 2, the ATD-PLL (Golestan et. al., 2017b) is presented, together with the corresponding small-signal modeling procedure. In Section 3, the novel ATD based QSG algorithm is presented, while in Section 4 the corresponding simulation results are outlined. In Section 5, the results of experimental tests are presented and analyzed.

2. REFERENCE SOLUTIONS

In this section, three reference solutions are presented. In Subsection 2.1 reference TD and ATD based solutions are outlined, accompanied by the ATD small signal model derivation, since the novel algorithm represents a modification of the ATD based PLL. In Subsection 2.2, a reference single-phase PLL algorithm with the input DC offset compensation is outlined, in order to outline the improvements introduced by the new algorithm.

2.1. Reference TD-PLL and ATD-PLL

The conventional TD-PLL (Golestan et. al., 2017a), based on the fixed time-delay QSG, is presented in the following Fig.1.

In Fig. 1, the TD-PLL consists of the following blocks and signals: the fixed T_r /4 time delay (where T_r represents the rated input signal period), block T $\alpha\beta$ to *dq* transformation, K_p and K_i the PLL proportional and integral gains, block I the PLL integral term, V_i PLL input signal, V_α and V_β input signal α and β components, V_q input signal *q* component, $\Delta\omega_e$ the PLL integrator output, ω_r rated input signal frequency, ω_e estimated frequency, and θ_e estimated phase angle value.

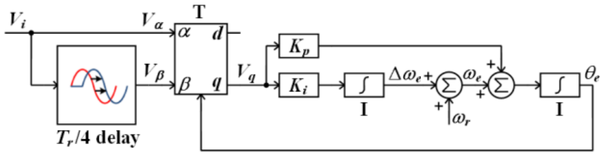


Fig.1. The conventional TD-PLL

The problem with the TD based QSG applied in a PLL resides in the fact that the input signal frequency ω_i differs from the presumed rated value ω_r, which results in the erroneous phase angle estimation and in the undesired double estimated frequency component in the V_q signal.

In order to solve this problem, the ATD-PLL (Golestan et. al., 2017b) in the following Fig. 2 is proposed, in which the modified adaptive TD based QSQ is applied. Namely, it still operates with the fixed time delay T_r/4, but, also, adaptively calculates the resulting orthogonal component V_β in order to compensate the error which occurs when the estimated input signal frequency ω_i does not correspond to the rated frequency value ω_r used for the time delay unit T_r calculation.

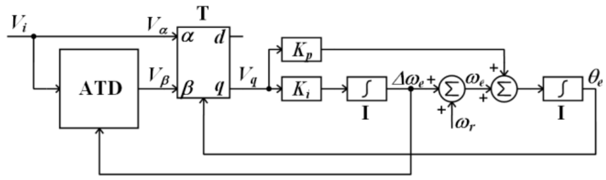


Fig. 2. The ATD based PLL (Golestan et. al., 2017b)

Namely, the signal $V_i(t) = V\cos(\omega_i t+\varphi_i) = V\cos(\theta_i)$ in Fig. 2 (where V represents the input signal amplitude, ω_i angular frequency, and φ_i phase angle values respectively) could be represented by means of orthogonal components $V_\alpha(t)$ and $V_\beta(t)$ by using the following equation (1).

$$\begin{bmatrix} V_i(t) \\ V_i(t-T_r/4) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \cos(\omega_i T_r/4) & \sin(\omega_i T_r/4) \end{bmatrix} \begin{bmatrix} V_\alpha(t) \\ V_\beta(t) \end{bmatrix} \quad (1)$$

Based on (1), the following QSG equation (2) can be derived,

$$V_\beta(t) = \frac{V_i(t-T_r/4) - V_i(t)\cos(\omega_i T_r/4)}{\sin(\omega_i T_r/4)} \quad (2)$$

However, after substituting ω_i with its estimated value ω_e, and ω_e with $\omega_e = \Delta\omega_e + \omega_r$ in (2) (where ω_r represents the rated value of the input signal frequency

ω_i, where the employed time delay unit T_r is equal to $T_r = 2\pi/\omega_r$, and where ω_e represents the ω_i value estimated by a PLL algorithm) the following equation (3) is obtained.

$$V_\beta(t) = \frac{V_i(t - T_r/4) + V_i(t)\sin(\Delta\omega_e T_r/4)}{\cos(\Delta\omega_e T_r/4)} \tag{3}$$

Consequently, by applying (3) for the QSG in ATD-PLL inf Fig. 2 the problem related to the undesired double-frequency component in estimated frequency and phase angle (caused by the input frequency differing from the rated value) is solved.

However, this solution could further be improved since solution in Fig. 2 is not immune in relation to the DC offset present at the PLL input, which could be solved by accordingly modifying the ATD-PLL algorithm.

Furthermore, the positive and negative sequence component separation based three-phase PLL could be implemented based on the new modified ATD-PLL.

Consequently, the novel ATD-PLL is proposed in the following Section III, which includes the aforementioned improvements.

In the following part of this Subsection 2.1, the small-signal model derivation for the ADT based PLL (Golestan et. al., 2017b) is presented, since the similar technique is applied in the case of the novel modified ADT-PLL proposed in this paper.

The ATD-PLL small-signal model is derived by means of the following equation (4), and by using (3) with $\Delta\omega_i = \omega_i - \omega_r$, $\Delta\theta_e = \theta_e - \omega_r t$, and $\Delta\theta_i = \theta_i - \omega_r t$.

$$\begin{aligned}
V_q(t) &= -\sin(\theta_e)V_\alpha(t) + \cos(\theta_e)V_\beta(t) \\
&= -V\sin(\theta_e)\cos(\theta_i) + \cos(\theta_e)\frac{V_i\left(t - \frac{T_r}{4}\right) + V_i(t)\sin\left(\frac{\Delta\omega_e T_r}{4}\right)}{\cos\left(\frac{\Delta\omega_e T}{4}\right)} \\
&= \frac{V}{2}\left[\sin(\theta_i - \theta_e) + \frac{\sin\left(\theta_i - \theta_e - \frac{\Delta\omega_i T_r}{4}\right)}{\cos\left(\frac{\Delta\omega_e T_r}{4}\right)} + \tan\left(\frac{\Delta\omega_e T_r}{4}\right)\cos(\theta_i - \theta_e)\right] \\
&\quad + \underbrace{\frac{V}{2}\left[-\sin(\theta_i + \theta_e) + \frac{\sin\left(\theta_i + \theta_e - \frac{\Delta\omega_i T_r}{4}\right)}{\cos\left(\frac{\Delta\omega_e T_r}{4}\right)} + \tan\left(\frac{\Delta\omega_e T_r}{4}\right)\cos(\theta_i + \theta_e)\right]}_{D_2(t)}
\end{aligned} \tag{4}$$

Since for $x \approx 0$, $\theta_i \approx \theta_e$, $\Delta\omega_i \approx 0$ and $\Delta\omega_e \approx 0$ the following terms are equal to $\sin(x) \approx x$, $\cos(x) \approx 1$, $\tan(x) \approx x$, and $D_2(t) \approx 0$, the small signal model (5) can be derived from (4).

$$V_q(t) \approx V\left[\frac{\Delta\theta_i + (\Delta\theta_i - \Delta\omega_i T_r/4)}{2} - \Delta\theta_e + \frac{\Delta\omega_e T_r}{8}\right] \tag{5}$$

After taking the Laplace transform of (5), the following small-signal transfer function (6) is obtained for the ADT based QSG.

$$V_q(s) \approx V\left[\frac{1 + e^{-sTr/4}}{2}\Delta\theta_i(s) - \Delta\theta_e(s) + \frac{\Delta\omega_e(s)T_r}{8}\right] \tag{6}$$

Consequently, based on (6), in (Golestan et. al., 2017b) the closed-loop transfer function of ATD-PLL in Fig. 3 is derived, accompanied by the corresponding PLL parameter tuning procedure.

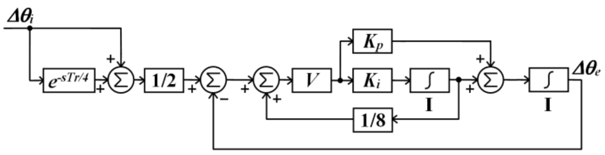
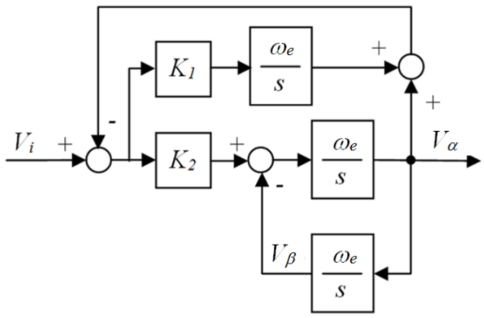


Fig. 3. The equivalent transfer function of the ADT-PLL small-signal model

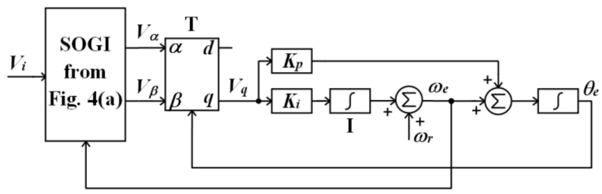
In order to enable the comparative analysis of the input DC offset rejection performed by the modified ATD-PLL proposed in this paper, in the following Subsections 2.2 and 2.3 two reference single-phase PLL algorithms are presented that include the DC offset compensation.

2.2. Single-phase SOGI based PLL algorithm with DC offset compensation

In (Karimi-Ghartemani et. al. 2012), the SOGI based single-phase PLL algorithm is proposed, with the DC offset compensation based on the additional integrator included in the QSG section, outlined in Fig. 4(a). In Fig. 4(b), the corresponding PLL algorithm is outlined.



(a)



(b)

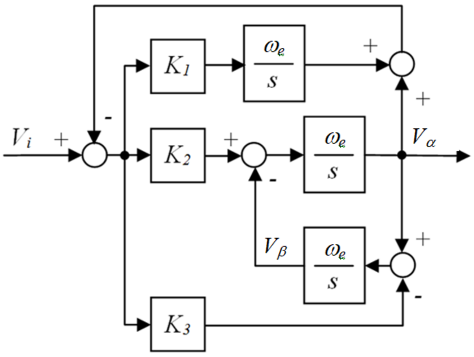
Fig. 4. The SOGI based (a) QSG, and (b) corresponding PLL with DC offset compensation (Karimi-Ghartemani et. al. 2012)

In (Karimi-Ghartemani et. al. 2012), the QSG parameter values are set to the values $K_1 = 75 / \omega_r = 0.239$ and $K_2 = 300 / \omega_r = 0.955$, for $\omega_r = 2\pi 50$ rad/s. The corresponding

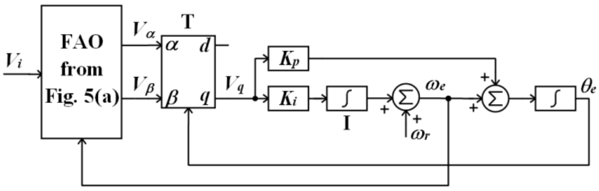
PLL parameter values are determined in the following Subsection 2.3.

2.3. Frequency adaptive observer based single-phase PLL algorithm with DC offset compensation

In (Park et. al., 2017), a second reference single-phase PLL algorithm with DC offset compensation is addressed, outlined in the following Fig. 5.



(a)



(b)

Fig. 5. The frequency adaptive observer-based (a) QSG, and (b) corresponding PLL with DC offset compensation (Park et. al., 2017)

In Fig. 5(a), the frequency adaptive observer-based (FAO) QSG is outlined. It is shown in (Park et. al., 2017) that FAO enables QSG with DC offset rejection that operates with improved dynamic responses. Namely, for the following set of FAO parameter values K_1 = 1, K_2 =2 and K_3 =2, the QSG with bandwidth BW = ω_e and dominant poles damping factor $\zeta = 1$ is obtained, which, according to (Park et. al., 2017), represents an improvement when compared with previously existing solutions. In Fig. 5(b), the corresponding PLL algorithm is outlined based on the QSG in Fig. 5(a).

The parameter values K_p and K_i for PLL algorithms in figures 4(b) and 5(b) are calculated by means of the procedure outlined in (Park et. al., 2017), which results in $K_p = 2\zeta\omega_0$ and $K_i = \omega_0^2$, where ζ and ω_0 represent PLL resulting dominant closed-loop poles damping factor and undamped angular frequency values (with ω_0 being approximately equal to the PLL bandwidth frequency value).

In the following Section 3, the novel modified ATD based PLL is outlined, which enables the input DC offset compensation.

3. THE MODIFIED ATD-PLL WITH DC OFFSET COMPENSATION

The main contribution proposed in this paper consists of the modification which enables ATD algorithm outlined in Fig. 2 to operate with a DC offset in the input signal. Namely, for the DC offset present at the PLL input the V_i signal can be represented by $V_i(t) = V\cos(\omega_i t+\varphi_i) + C = V\cos(\theta_i) + C$, where C represents the DC offset signal. Consequently, similarly to (2), the $V_i(t)$ can be represented with the corresponding orthogonal components $V_\alpha(t)$ and $V_\beta(t)$ by means of the following equation (7).

$$\begin{bmatrix} V_i(t) \\ V_i(t-T_r/4) \\ V_i(t-T_r/2) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ \cos(\omega_i T_r/4) & \sin(\omega_i T_r/4) & 1 \\ \cos(\omega_i T_r/2) & \sin(\omega_i T_r/2) & 1 \end{bmatrix} \begin{bmatrix} V_\alpha(t) \\ V_\beta(t) \\ C \end{bmatrix} \tag{7}$$

Based on (7), the following QSG equations (8) and (9) can be derived by substituting ω_i with its estimate ω_e, and ω_e with $\omega_e = \Delta\omega_e + \omega_r$ (where ω_r represents the rated value of the input signal frequency ω_i, where the employed time delay unit T_r is equal to $T_r = 2\pi/\omega_r$, and where ω_e represents the ω_i value estimated by a PLL algorithm).

$$V_\alpha(s) = \frac{V_i(t)\left[1+2\sin\left(\frac{\Delta\omega_e T_r}{4}\right)\right] - 2V_i(t-T_r/4)\sin\left(\frac{\Delta\omega_e T_r}{4}\right) - V_i(t-T_r/2)}{2\left[\sin\left(\frac{\Delta\omega_e T_r}{4}\right)+1\right]} \tag{8}$$

$$V_\beta(s) = -\frac{V_i(t)\left[1-2\sin\left(\frac{\Delta\omega_e T_r}{4}\right)\right] - 2V_i(t-T_r/4)\left[1-\sin\left(\frac{\Delta\omega_e T_r}{4}\right)\right] + V_i(t-T_r/2)}{2\cos\left(\frac{\Delta\omega_e T_r}{4}\right)} \tag{9}$$

In the following subsection, the small-signal model of the proposed QSG and PLL technique is outlined.

3.1. The novel ATD-PLL small-signal model

The small-signal model of the ADT-PLL in Fig. 6 is derived from the small-signal approximation of the signal $V_q(t)$= -sin(θ_e)$V_\alpha(t)$ + cos(θ_e)$V_\beta(t)$, and $V_\alpha(t)$ and $V_\beta(t)$ outlined in (8) and (9). Consequently, the following equation (10) is obtained, for $\Delta\omega_i = \omega_i - \omega_r$, $\Delta\theta_e = \theta_e - \omega_r t$, and $\Delta\theta_i = \theta_i - \omega_r t$.

Since for $x \approx 0$, $\theta_i \approx \theta_e$, $\Delta\omega_i \approx 0$ and $\Delta\omega_e \approx 0$ the following terms are equal to $\sin(x) \approx x$, $\cos(x) \approx 1$, $\tan(x) \approx x$, and $D(t) \approx 0$, the resulting novel ATD small-signal model (11) can be derived from (10).

$$V_q(t) = -\sin(\theta_e)V_\alpha(t) + \cos(\theta_e)V_\beta(t)$$
$$= \frac{V}{2}\frac{\left\{\sin(\theta_i-\theta_e)\left[1+2\sin\left(\frac{\Delta\omega_e T_r}{4}\right)\right]+2\cos\left(\theta_i-\theta_e-\frac{\Delta\omega_i T_r}{4}\right)\sin\left(\frac{\Delta\omega_e T_r}{4}\right)+\sin\left(\theta_i-\theta_e-\frac{\Delta\omega_i T_r}{2}\right)\right\}}{2\left[\sin\left(\frac{\Delta\omega_e T_r}{4}\right)+1\right]}$$
$$-\frac{V}{2}\frac{\left\{\cos(\theta_i-\theta_e)\left[1-2\sin\left(\frac{\Delta\omega_e T_r}{4}\right)\right]-2\sin\left(\theta_i-\theta_e-\frac{\Delta\omega_i T_r}{4}\right)\left[1-\sin\left(\frac{\Delta\omega_e T_r}{4}\right)\right]-\cos\left(\theta_i-\theta_e-\frac{\Delta\omega_i T_r}{2}\right)\right\}}{2\cos\left(\frac{\Delta\omega_e T_r}{4}\right)}$$
$$+D(t) \quad (10)$$

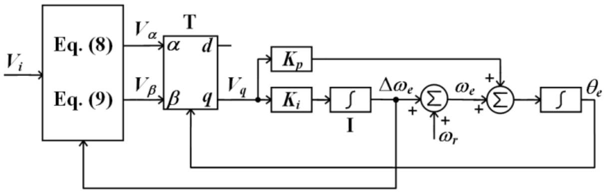


Fig. 6. The novel ATD-PLL with DC offset compensation

$$V_q(t) \approx V\left[\frac{\Delta\theta_i + (\Delta\theta_i - \Delta\omega_i T_r/2)}{2} - \Delta\theta_e + \frac{\Delta\omega_e T_r}{4}\right] \quad (11)$$

After taking the Laplace transform of (11), the following small-signal model transfer function (12) is obtained for the novel ATD based QSG, outlined in Fig. 5.

$$V_q(s) \approx V\left[\frac{1+e^{-sTr/2}}{2}\Delta\theta_i(s) - \Delta\theta_e(s) + \frac{\Delta\omega_e(s)T_r}{4}\right] \quad (12)$$

Based on (12), the small-signal model of a novel ATD based PLL from Fig. 6 is outlined in the following Fig. 7.

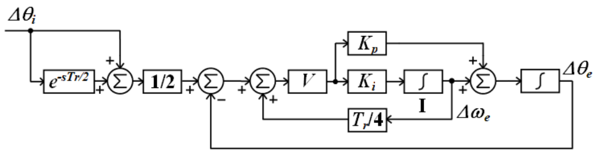


Fig. 7. The novel ATD-PLL small signal model

In the following Subsection 3.2, the novel ATD-PLL parameter tuning procedure is outlined.

3.2. The novel ATD-PLL parameter tuning procedure

The novel ATD-PLL parameter tuning procedure is derived from the small-signal model outlined in Fig. 6. Namely, based on the model, the following closed-loop transfer function (13) is obtained.

$$G_{pll}(s) = \frac{\Delta\theta_e(s)}{\Delta\theta_i(s)} = \frac{1+e^{-sTr/2}}{2}\frac{V(K_p s + K_i)}{s^2 + V(K_p - T_r K_i/4)s + VK_i} \quad (13)$$

The ATD-PLL dynamic performance characteristics are set by means of parameter values K_p and K_i, by tuning the zero placement of the characteristic polynomial $D_{pll}(s) = s^2 + V(K_p - T_r K_i/4)s + VK_i$ of the transfer function (13).

Namely, since the $D_{pll}(s)$ represents a second order polynomial, the resulting PLL dynamic characteristics are determined by the required $D_{pll}(s)$ zeros damping ratio ζ and undamped angular frequency ω_0 values (where ω_0 corresponds to the PLL closed-loop bandwidth value), which are outlined in the following equations (14)-(15).

$$2\xi\omega_0 = V(K_p - T_r K_i/4) \quad (14)$$
$$\omega_0^2 = VK_i \quad (15)$$

From (14)-(15) following equations (16) and (17) are derived for the PLL parameter values Kp and Ki.

$$K_i = \frac{\omega_0^2}{V} \quad (16)$$
$$K_p = \frac{2\xi\omega_0}{V} + \frac{T_r\omega_0^2}{4V} \quad (17)$$

Based on (16)-(17) it can be concluded that the dynamics of the novel ATD-PLL with DC offset compensation can be tuned freely with respect to the input signal rated frequency value ω_r, which is not the case in the most existing solutions, including the FAO and SOGI based reference solutions outlined in figures 4 and 5.

In the following Section 4, the results of simulation tests are presented for the novel and for the reference PLL solutions.

4. SIMULATION TESTS

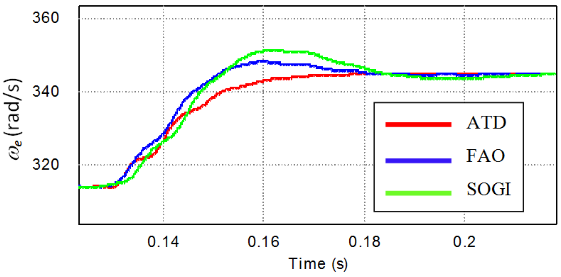
Since the main contribution proposed in this paper consists of the single-phase ATD-PLL modification that enables the input signal DC offset compensation, in this section the novel solution is compared with the reference FAO and SOGI based PLL solutions outlined in figures 4 and 5. Two different PLL applications are investigated – the basic single-phase PLL with DC offset in the input signal, and the three-phase PLL application with the positive and negative sequence separation for the nonsymmetrical PLL input signals.

4.1. Simulation tests of single-phase PLL applications with the DC offset compensation

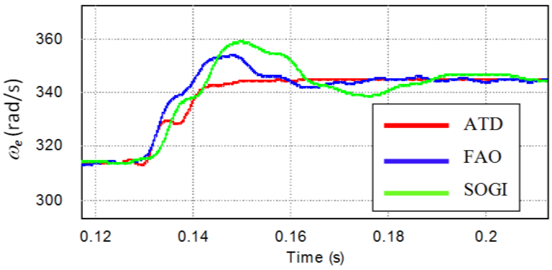
For the simulation of SOGI based PLL in Fig. 4(b) the following set of parameters are used (Karimi-Ghartemani et. al. 2012): K_1 = 0.239 and K_2 = 0.955. For the simulation of FOA in Fig. 5(b) the following set of parameters are used (Park et. al., 2017): K_1 = 1, K_2 =2 and K_3 =2. The PLL PI loop filter parameters are determined by using $K_p = 2\zeta\omega_0$ and $K_i = \omega_0^2$, for $\zeta = 1$ and for ω_0 equal to the required PLL bandwidth value.

For the novel ATD-PLL in Fig. 6 the PI loop filter parameters are determined by means of (14)-(15).

In the first set of simulation test three examined PLL structures are simulated for the following two different PLL bandwidth frequency values ω_0 - 150 rad/s and 300 rad/, for input frequency step variations equal to 31 rad/s.



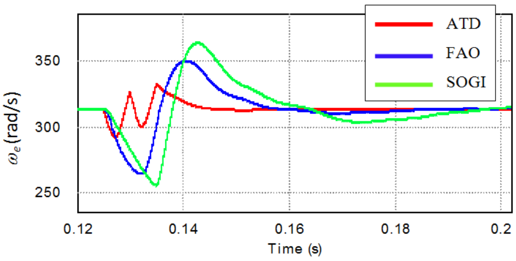
(a)



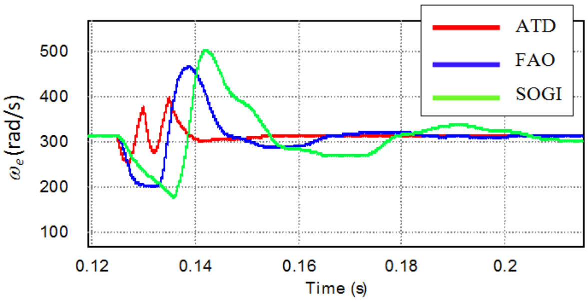
(b)

Fig. 8. Simulated estimated frequencies of three single-phase PLLs, for 31 rad/s input frequency step variations, rated frequency ωr = 314 rad/s, for PLL bandwidth frequency (a) ω0 = 150 rad/s and (b) ω0 = 300 rad/s

By analyzing traces in Fig. 8(a) it can be concluded that for lower bandwidth frequency BW = 150 rad/s for all three examined PLLs similar settling times $t_{set} \approx 50$ ms are achieved, while the new ATD-PLL operates without any overshoot, contrary to two other solutions. However, the clear advantage of the new ATP-PLL can be observed in the traces in Fig. 8(b) for BW = 300 rad/s, where the new ATD based solution operates with no overshoot o_1 = 0%, and with the fastest settling time t_{set1} = 20 ms, while FAO operates with t_{set2} = 43 ms and o_2 = 30%, and SOGI with t_{set3} = 78 ms and o_3 = 45%.



(a)



(b)

Fig. 9. Simulated estimated frequencies for three examined single-phase PLLs, for input step offset equal to 1V, rated frequency ωr = 314 rad/s, and for (a) PLL BW = 150 rad/s, and (b) BW = 300 rad/s

By analyzing traces in Fig. 9 it can be concluded that the same set of corresponding settling times are achieved as in the traces in Fig. 8, which furthermore illustrates the improvement introduced by the new ATD based PLL.

4.2. Simulation tests of three-phase PLL applications with the DC offset compensation and with the positive sequence component separation

The three-phase PLL with DC offset compensation and positive sequence separation is examined in this paper due to its wide scope of applications in the power converters design.

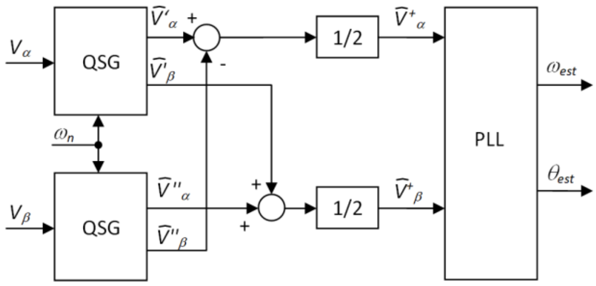
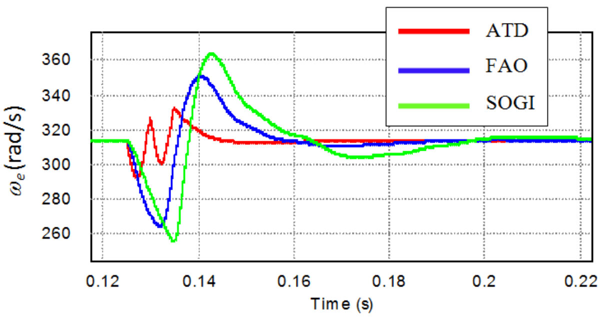
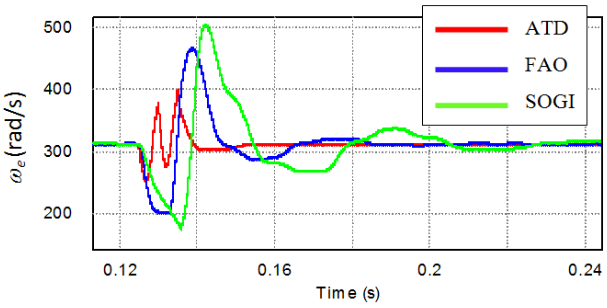


Fig. 10. Conventional three-phase PLL with positive sequence separation

In Fig. 10, a conventional three-phase application for the positive sequence application is outlined, where the QSG section can be implemented by means of the novel ATD in equations (8) and (9), SOGI in Fig. 4(a), and FAO in Fig. 5(a).



(a)



(b)

Fig. 11. Simulated estimated frequencies for three examined three-phase PLLs with positive sequence separation, for input step offset equal to 1V, rated frequency ωr = 314 rad/s, and for (a) PLL BW = 150 rad/s, and (b) BW = 300 rad/s

By analyzing simulation traces in Fig. 11 the following conclusions are made: (a) for BW = 150 rad/s in Fig. 11(a) settling times are t_{set1} = 20 ms for the new ATD, t_{set2} = 44 ms for FAO, and t_{set3} = 68 ms for SOGI; (b) for BW = 300 rad/s in Fig. 11(b) settling times are t_{set1} = 20 ms for the new ATD, t_{set2} = 53 ms for FAO, and t_{set3} = 90 ms for SOGI. Furthermore in both cases in figures 11(a) and 11(b) the smallest overshot is achieved for the new ATD based PLL.

Consequently, simulation results in Fig. 11 illustrate a clear advantage of the new ATD based PLL with the DC offset compensation and positive sequence separation when compared with the similar solutions based on FAO and SOGI.

3. EXPERIMENTAL TESTS

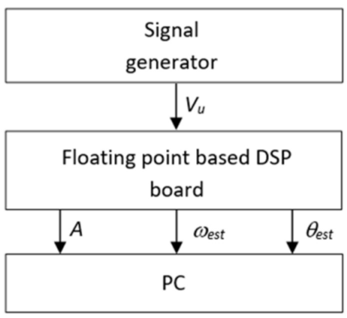
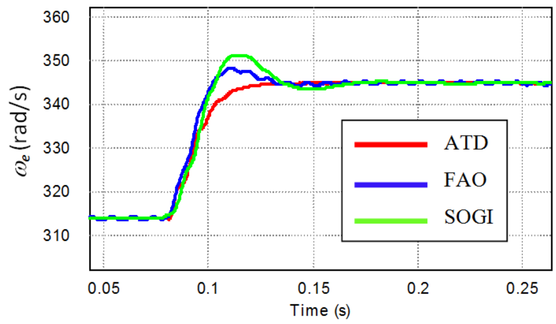
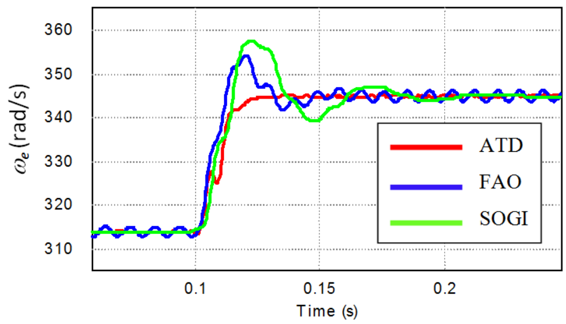


Fig. 12. Experimental setup

In Fig. 12, the outline of the experimental setup is presented, which is employed in this paper. The signal generator is used to generate a single-phase power grid signal. For the experiments that include positive sequence component separation, a nonsymmetrical voltage system is fed into the PLL by introducing a zero voltage at the corresponding V_β input.

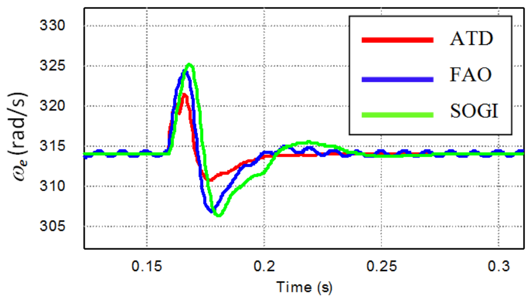


(a)

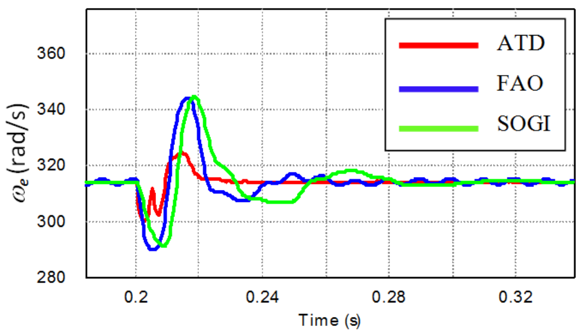


(b)

Fig. 13. Experimental estimated frequencies of three single-phase PLLs, for 31 rad/s input frequency step variations, rated frequency ωr = 314 rad/s, for PLL bandwidth frequency (a) ω0 = 150 rad/s and (b) ω0 = 300 rad/s

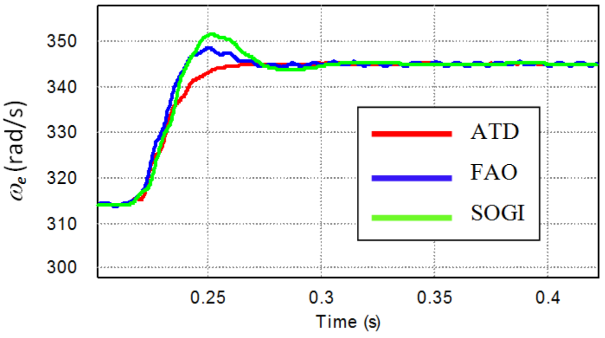


(a)

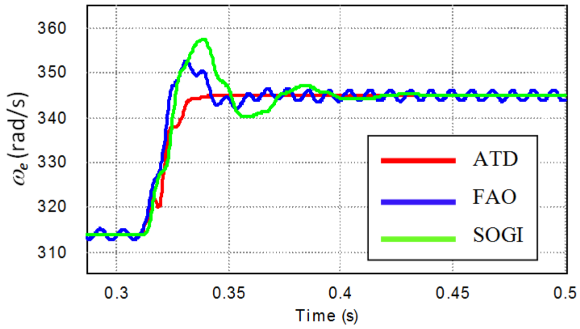


(b)

Fig. 14. Experimental estimated frequencies for three single-phase examined PLLs, for input step offset equal to 0.25V, rated frequency ωr = 314 rad/s, and for (a) PLL BW = 150 rad/s, and (b) BW = 300 rad/s

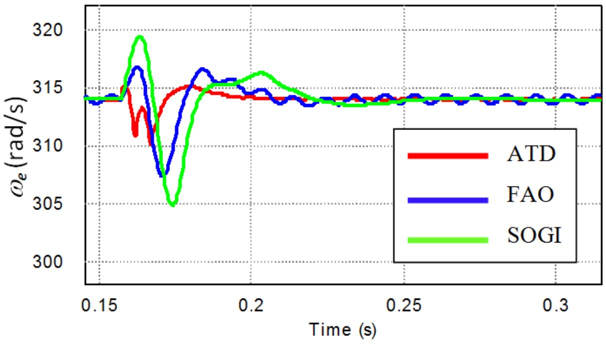


(a)

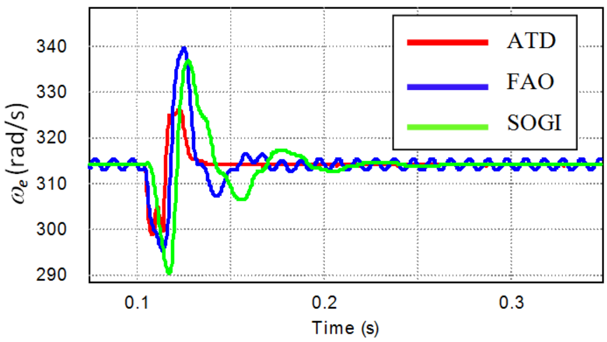


(b)

Fig. 15. Experimental estimated frequencies for three examined three-phase PLLs with positive sequence separation, for input frequency 31 rad/s step variation, rated frequency ωr = 314 rad/s, and for (a) PLL BW = 150 rad/s, and (b) BW = 300 rad/s



(a)



(b)

Fig. 16. Experimental estimated frequencies for three examined three-phase PLLs with positive sequence separation, for input DC offset 0.25 V setp variation, rated frequency ωr = 314 rad/s, and for (a) PLL BW = 150 rad/s, and (b) BW = 300 rad/s

In figures 13 and 14 experimental results of the estimated frequency values for single-phase PLL implementations are presented, performed for three different QSG algorithms (SOGI, FAO, and new ATD) designed for two different bandwidth frequency values – 150 rad/s and 300 rad/s. In Fig. 13, input signal 31 rad/s frequency variations are performed, while in Fig. 14 input signal DC offset 0.25 V step variations are introduced. Consequently, similar estimated frequency response overshoot and settling times are obtained as in the corresponding simulation tests (Fig. 8 corresponds to Fig. 13, and Fig. 9 corresponds to Fig. 14).

In figures 15 and 16 experimental test results are outlined for the three-phase PLLs with positive sequence separation, implemented with three different QSG algorithms (SOGI, FOA, and new ATD) designed for two bandwidth frequencies – 150 rad/s and 300 rad/s. Experiments include input signal step frequency variations in Fig. 15, and input signal DC offset variations in Fig. 16, where the similar overshoot and settling times are obtained as in the corresponding simulation test outlined in Fig. 11. Consequently, based on the results of experimental test, similarly as in the case of the simulation tests, it can be concluded that the new ATD based PLL with DC offset compensation enables the phase and frequency synchronization responses with significantly lower overshoot and settling time values.

6. CONCLUSIONS

In this paper, a new ATD based PLL application is presented, which enables input signal DC offset compensation. The new PLL is based on the modified ATD based QSG algorithm, which is applied in the paper by two different means – in a single-phase, and in the three-phase PLL application with the positive sequence separation. Proposed novel QSG algorithm is accompanied by a corresponding small-signal model, and by the PLL parameter tuning procedure based on the derived PLL model. Paper, also, includes, the simulation and experimental tests used to compare the novel ATD algorithm with two reference solutions existing in the literature – SOGI, and FAO. Obtained results show that the novel ATD based QSG enables PLL operation with significantly reduced overshoot and settling times for the PLL applications designed for the same bandwidth frequency values.

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