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Fixed time control based on finite time observer for Buck converter system with load disturbance

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Abstract: To improve transient response and reduce current ripple, a fixed time voltage regulation control strategy based on finite time observer for Buck converter is proposed in this paper. Different from the previous methods of adding additional circuits, the proposed fixed time controller combined with load finite time observer can be directly applied in integrated circuits. Meantime it avoids the chatter and vibration of sliding mode control strategy, relaxing constraint on initial condition of finite time control strategy. Firstly, a finite time observer is designed to estimate the uncertain load resistance. Secondly, combined with the backstepping method, a fixed time voltage regulation control strategy is designed by fixed time control theory, so that the output voltage has a credible ability to converge to the reference voltage in a fixed time. Finally, the proposed control strategy is verified by comparing with the finite time controller and sliding mode controller, where the obtained simulation and experiment results show the proposed strategy can make better performance in terms of convergence speed and ripple reduction when the reference voltage and the load change.

Keywords: Buck converter, finite time observer, fixed time control, fast response, backstepping method.

1. INTRODUCTION

As the basic topology structure of DC-DC converter, Buck converter is widely used in electric vehicle, aerospace engineering, home electronics and other fields. For occasions with high real-time requirements, it is urged to consider the transient response in addition to power conversion efficiency. Due to the non-linearity of Buck converter itself, traditional linear methods are difficult to be applied in practice. Moreover, the load changes slowly over time, making the model information not accurate and leading to the failure of the control strategy. It is necessary to investigate the approaches to improve the transient response of Buck converter.

There exist two main methods, additional circuit and nonlinear control, to improve the transient response of the Buck converter.

To realize fast transient response, some additional auxiliary switches are added to change the equivalent output inductance (Gu et al., 2014). To track the output voltage of Buck converter, an additional auxiliary converter is designed as the load changes (Jia et al., 2013). The authors (Hsu et al., 2019) adds an error amplifier to the pulse width modulation (PWM) circuit to achieve transient response by accelerating the output level drift of the error amplifier. However, the driving ability is related to the size of the external transistor. To obtain sufficient driving ability, a certain scale of area of chips has to be occupied forcibly. To acquire fast transient response, limiting error amplifier and fast error signal control are utilized (Zeng et al., 2019). Thus, limited by size and cost, more and more researchers are focusing on improving the transient response of Buck converter with nonlinear control methods. Finite time control (Wen et al., 2021; Shihua et al., 2016; Wang et al., 2017; Zhang et al., 2020; Du et al., 2019)and sliding

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mode control (Goudarzian et al., 2020; Fu et al., 2020; Shi et al., 2020; Cheng et al., 2020; Wang et al., 2020) are mainly used. Based on finite time control technique, a fast control strategy for Buck converter is proposed to make the output voltage converges to the reference voltage in finite time (Wen et al., 2021; Shihua et al., 2016; Wang et al., 2017; Zhang et al., 2020), where the upper bound of convergence time is related to the initial state. As the initial state of the system changes, the upper bound of convergence time also changes correspondingly. In order to achieve current sharing in parallel Buck circuits, a finite time flow-sharing control algorithm is proposed to improve ability of tracking the reference voltage and robustness to load disturbances (Du et al., 2019). With the application of sliding mode control methods, many researchers have started to use sliding mode control to improve the response speed of Buck converter. A digital fast terminal sliding mode control method is studied for Buck converter with mismatched interference, which has high accuracy for tracking voltage and great dynamic characteristics under different working conditions (Goudarzian et al., 2020). In (Fu et al., 2020), an adaptive nonsingular terminal sliding mode control strategy for bi-directional DC-DC converters in hybrid energy storage systems is proposed to allow errors between output voltage and reference voltage to converge quickly in a limited time compared with the second-order sliding mode controller. In (Shi et al., 2020), to improve the performances of fast transient response, a sliding mode control combined with fixed time control is proposed. However, in the actual sliding mode control (Goudarzian et al., 2020; Fu et al., 2020; Shi et al., 2020; Cheng et al., 2020; Wang et al., 2020), due to the uncertainty of the model and the existence of interference, chattering phenomenon and steady-state error always exist and lead to adverse effects.

It is worth pointing out that there are three urgent considerations in the above methods to improve the transient response of Buck converter.

Firstly, the aforementioned increased circuit structures generally increase cost or volume, which is difficult to be applied in integrated circuits. Finite time control is related to the initial state of the system, and the convergence speed cannot meet the real-time requirements. Sliding mode control has a frightening problem of chattering, which makes the stability requirement of electric vehicles and other occasions difficult to be satisfied.

Secondly, in the above researches, less attention is paid to the ripple in the circuit. The transient response of the load is affected by the equivalent output inductance. The smaller the inductance, the faster the transient response. However, reducing the equivalent inductance will increase the current ripple and reduce the efficiency of the converter (Wang et al., 2019), which could lead to shorting the service life of the capacitor. There are many researches on ripple suppression of Buck converter (Wang et al., 2019; Cao et al., 2020; Yan et al., 2018), but the applied methods is by changing the circuit structure, which is difficult to realize.

Thirdly, most of the above researches need to establish accurate converter state space model. In the actual system, external loads tend to change with time. Because accurate system parameters are often not available, this results into an undesirable transient response. Therefore, some scholars have carried out researches on finite time observer. For the Buck converters without current signal, the finite time output feedback controller based on the observer is designed by using finite time control method and observer technology, which ensures that the system converges to the equilibrium state in a finite time (Du et al., 2014). A non-smooth current constrained control algorithm is proposed for Buck converters with uncertain parameters . This control algorithm prevents transient current from being too large by sacrificing the transient performance of the system (Miao et al., 2020). The control methods of disturbance observer and non disturbance observer are analyzed and compared, whose results show that the control strategy with disturbance observer has greater advantages in anti-interference (Yin et al., 2020). To ensure that the state of the system is still bounded even in the presence of faults, an adaptive finite time controller based on output feedback combined with a fuzzy observer is designed (Wang et al., 2022). The above researches make the application of the observer in Buck converter achieve well performance in voltage tracking and load adaption. However, the above researches do not take into account combining the finite time observer with fixed time controller. The combination of advantages lies in two aspects: (a) the finite time observer can quickly track the load disturbance; (b) the fixed time controller is independent of the initial state parameters of the system, further improving the convergence speed and anti-interference ability.

Therefore, in this paper, a composite control strategy is proposed by combining fixed time technique with a finite time observer. The main innovations of the paper can be summarized as follows:

(1) To improve the transient response and anti-interference of the system, the combination of finite time observer and fixed time controller is designed, where the finite time observer is used to accurately estimate load disturbance and the fixed time controller is used to further improve the convergence rate of the system.

(2) Compared with (Shi et al., 2020), the fixed time controller based on backstepping technology is designed to avoid chattering, where the proposed strategy reduces circuit size and hardware cost.

(3) To verify the convergence rate of the proposed method, the comparison with sliding mode controller (Cheng et al., 2020) and finite time controller (Zhang et al., 2020) are given, whose results show that the proposed fixed time controller can effectively improve response speed and reduce current ripple.

The rest of this paper is organized as follows. System description and preliminary knowledge are shown in Section 2. Design of the fixed time controller with load finite time observer is given in Section 3. A finite time controller for comparison is designed in Section 4. Simulation and experiment results are presented in Section 5. The conclusions are drawn in Section 6.

2. SYSTEM DESCRIPTION AND PRELIMINARY KNOWLEDGE

2.1 Model description of Buck converter

The model of Buck DC-DC converter based on fixed time controller is shown in Fig. 1, where V_o is the output voltage; V_{in} is the input voltage; V_{ref} is the reference voltage; i_C is the output capacitor current; i_L is the inductance current; S_w is the switching element of MOSFET(Metal-Oxide-Semiconductor Field-Effect Transistor); D is a freewheeling diode; C is the output capacitance; L is the input inductance; R is the load resistance; $\hat{R}$ is the estimate of R; u is the controller output; x_1 is the output voltage error and x_2 is the i_C.

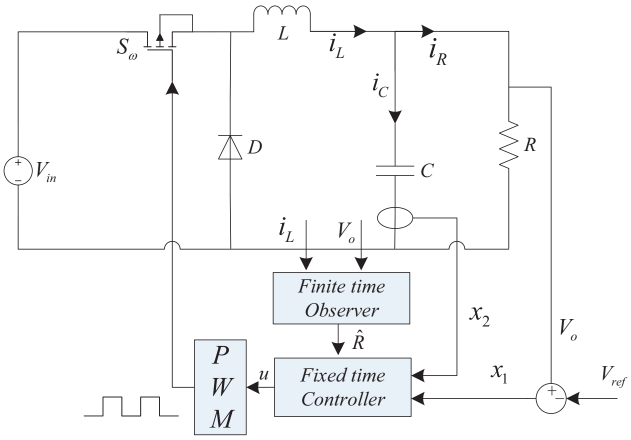

Fig. 1. Buck converter based on fixed-time controller.

When the switch turns on, the state space equation of the system is given as (Zhang et al., 2020)

$$\begin{cases} \dfrac{di_C}{dt} = \dfrac{V_{in} - V_o}{L} - \dfrac{\dot{V}_o}{R}, \\ \dfrac{dV_o}{dt} = \dfrac{i_C}{C}. \end{cases} \tag{1}$$

When the switch turns off, the state space equation of the system is given as (Zhang et al., 2020)

$$\begin{cases} \dfrac{di_C}{dt} = -\dfrac{V_o}{L} - \dfrac{\dot{V}_o}{R}, \\ \dfrac{dV_o}{dt} = \dfrac{i_C}{C}. \end{cases} \tag{2}$$

According to (1) and (2), the average model of Buck converter in continuous conduction mode is expressed as

$$\begin{cases} \dot{V}_o = \dfrac{1}{C} i_C, \\ \dot{i}_C = \dfrac{uV_{in} - V_o}{L} - \dfrac{\dot{V}_o}{R}. \end{cases} \tag{3}$$

Assuming that V_{ref} is the expected reference output voltage, we have

$$\begin{cases} \dot{x}_1 = \dfrac{x_2}{C}, \\ \dot{x}_2 = -\dfrac{x_1}{L} - \dfrac{x_2}{RC} - \dfrac{V_{ref}}{L} + \dfrac{V_{in}}{L} u, \end{cases} \tag{4}$$

where $x_1 = V_o - V_{ref}$ and $x_2 = i_C$.

Our purpose is to design a controller to ensure that the output voltage error of the system (4) converges to 0 in a fixed time.

2.2 Preliminary knowledge

Lemma 1 (Li et al., 2020) : If there exists a continuous radially unbounded and positive definite function $V(x)$ such that

$$\dot{V}(x) \leq -\eta V(x)^{\bar{p}} \tag{5}$$

where $\bar{p} \in (0, 1)$, $\eta > 0$, then the zero solution $x(t) \equiv 0$ to (4) is finite time stable.

Lemma 2 (Chen et al., 2021) : If there exists a continuous radially unbounded and positive definite function $V(x)$ such that

$$\dot{V}(x) \leq -\sigma V(x)^{\upsilon_1} - \delta V(x)^{\upsilon_2} \tag{6}$$

where $\sigma > 0, \delta > 0, 0 < \upsilon_1 < 1, \upsilon_2 > 1$, then the origin of the system (4) is globally fixed time stable and the settling time function T can be estimated by

$$T \leq T_{\max} := \frac{1}{\sigma(1 - \upsilon_1)} + \frac{1}{\delta(\upsilon_2 - 1)}. \tag{7}$$

Furthermore, if $\upsilon_1 = 1 - \frac{1}{\upsilon_3}$ and $\upsilon_2 = 1 + \frac{1}{\upsilon_3}$ with $\upsilon_3 > 1$ are selected, the settling time function T can be estimated by a less conservative bound

$$T_{\max} := \frac{\pi \upsilon_3}{2\sqrt{\sigma\delta}}. \tag{8}$$

Lemma 3 (Liu et al., 2021) (Cauchy-Schwartz inequality) : For any $j > 0$, i = 1,...,n, the following inequality holds

$$(\sum_{i=1}^{n} j_i)^2 \leq n \sum_{i=1}^{n} j_i^2. \tag{9}$$

Lemma 4 (Chen et al., 2021) (Young′s inequality) : For each pair $(g, f) \in R^2$, the following inequality holds

$$|g|\,|f| \leq \frac{\kappa^p}{p}|g|^p + \frac{1}{q\kappa^q}|f|^q \tag{10}$$

where $\kappa > 0$, $p > 1$, $q > 1$, $\frac{1}{p} + \frac{1}{q} = 1$.

Lemma 5 (Cheng et al., 2017): For the following observer system

$$\begin{cases} \dot{\phi}_1 = \varphi\phi_2 - \varphi r_1 |\phi_1|^{\rho_1} sign(\phi_1), \\ \dot{\phi}_2 = -\varphi r_2 |\phi_1|^{\rho_2} sign(\phi_1), \end{cases} \tag{11}$$

where $\varphi > 0$, $0.5 < \rho_1 < 1$, and $\rho_2 = 2\rho_1 - 1$, by choosing appropriate parameters r_1 and r_2, the observer system(11) state can be stabilized in a finite time.

3. DESIGN OF THE FIXED TIME CONTROLLER WITH LOAD FINITE TIME OBSERVER

The fixed time control based on finite time observer algorithm for the Buck converter system (4) is given in two steps:

(i) For load disturbances, a load finite time observer is proposed to estimate the load value in a finite time.

(ii) Based on the load value estimated by the observer, a fixed time control algorithm is proposed such that the reference voltage is tracked in a fixed time.

3.1 Design of the load finite time observer

In this section, the load finite time observer is designed. It is assumed that the system disturbance mainly originates from the load variation, while the inductance and capacitance are constants. In order to eliminate the effects of load disturbances, a load finite time observer is designed to estimate the value of the load and transmit the estimated value to the controller in real time.

Theorem 1 For the system (4) with an unknown load resistance, if the load observer is designed as

$$\begin{cases} \hat{V}_0 = \dfrac{1}{C}(i_L + \hat{\theta} V_0) + \upsilon_1 V_0 \left| V_0 - \hat{V}_0 \right|^{\eta_1} sign(V_0 - \hat{V}_0), \\ \dot{\hat{\theta}} = \upsilon_2 V_0 \left| V_0 - \hat{V}_0 \right|^{\eta_2} sign(V_0 - \hat{V}_0), \end{cases} \tag{12}$$

then the estimate value θ converges to the real value in a finite time, where $\upsilon_1 > 0, \upsilon_2 > 0$, $0.5 < \eta_1 < 1$, $\eta_2 = 2\eta_1 - 1$, and $\theta = -1/R$. $\hat{\theta}$ is the estimate of θ. $\hat{V}_0$ is the estimate of V_0.

Proof: The estimate error is designed as

$$\begin{cases} \phi_1 = V_0 - \hat{V}_0, \\ \phi_2 = \theta - \hat{\theta}. \end{cases} \tag{13}$$

As the resistance value varies slowly, we assume that its derivative is 0. Take the derivative of (13) and substitute it into (12) yields

$$\begin{cases} \dot{\phi}_1 = \dfrac{V_0}{C}\phi_2 - \upsilon_1 V_0 |\phi_1|^{\eta_1} sign(\phi_1), \\ \dot{\phi}_2 = -\upsilon_2 V_0 |\phi_1|^{\eta_2} sign(\phi_1). \end{cases} \tag{14}$$

Let $\varphi = \frac{V_0}{C}$, and substitute it into (14) yields

$$\begin{cases} \dot{\phi}_1 = \varphi\phi_2 - \upsilon_1 C\varphi |\phi_1|^{\eta_1} sign(\phi_1), \\ \dot{\phi}_2 = -\upsilon_2 C\varphi |\phi_1|^{\eta_2} sign(\phi_1). \end{cases} \tag{15}$$

According to **Lemma 5**, the observer system state (15) is stable in a finite time, which means that the estimated value converges to the real value in a finite time.

3.2 Design of the fixed time controller

In this section, the fixed time controller is designed. Firstly, changes of coordinates are introduced and the Lyapunov function is constructed. Then, the intermediate control rate is designed by the backstepping method. Finally, the suitable controller u is designed to satisfy the fixed time control theory.

According to the error dynamic system (4), we have

$$\begin{cases} \dot{x}_1 = a x_2, \\ \dot{x}_2 = -b x_1 - c x_2 - d + k u, \end{cases} \tag{16}$$

where $b = \frac{1}{L}$, $c = \frac{1}{RC}$, $d = \frac{V_{ref}}{L}$, $k = \frac{V_{in}}{L}$.

The system (16) is transformed by coordinating transformation, mainly to facilitate the parameter design of the controller.

The following changes of coordinates are introduced first

$$\begin{cases} z_1 = x_1, \\ z_2 = x_2 - \beta, \end{cases} \tag{17}$$

where β is the intermediate control law.

Theorem 2 For the transformed error system (17) , if the controller u is designed as

$$u = \frac{b x_1 + c x_2 + d + \dot{\beta} - m_3 - m_4 z_2^3 - \frac{a}{2} z_2}{k}, \tag{18}$$

then the state of the system converges to the origin in a fixed time.(Note:m_h is positive number(h =1,...,6).)

Proof: A backstepping method combined with fixed time control theory is employed.

Step 1: In this step, we design the virtual control signal β such that V_1 satisfies the following inequality

$$\dot{V}_1 \le \frac{a}{2} z_2^2 - m_1 V_1^{\frac{1}{2}} - m_2 V_1^2. \tag{19}$$

We design the Lyapunov functional candidate as

$$V = V_1 + V_2, \tag{20}$$

$$V_1 = \frac{1}{2} z_1^2, \tag{21}$$

$$V_2 = \frac{1}{2} z_2^2. \tag{22}$$

The derivative of (20) is

$$\dot{V} = \dot{V}_1 + \dot{V}_2. \tag{23}$$

The derivative of (21) is

$$\dot{V}_1 = z_1 \dot{z}_1 = z_1 z_2 a + z_1 a \beta. \tag{24}$$

By using **Lemma 4** inequality scaling, we have

$$\dot{V}_1 \le \frac{a}{2} z_1^2 + \frac{a}{2} z_2^2 + z_1 a \beta. \tag{25}$$

The virtual control signal β is designed as follows

$$\beta = -\frac{1}{2} z_1 - \frac{m_1}{a} - \frac{m_2}{a} z_1^3. \tag{26}$$

The derivative of (26) is

$$\dot{\beta} = -\frac{1}{2}\dot{z}_1 - \frac{m_2}{a} z_1^2 \dot{z}_1. \tag{27}$$

By substituting (26) into (25), we have

$$\begin{aligned} \dot{V}_1 &\le \frac{a}{2} z_2^2 - m_1 z_1 - m_2 z_1^4 \\ &= \frac{a}{2} z_2^2 - m_1 V_1^{\frac{1}{2}} - m_2 V_1^2. \end{aligned} \tag{28}$$

Step 2: In this step, we design the u to satisfy the fixed time control theorem.

By Substituting $\dot{V}_1$ obtained in step 1 into (23), we have

$$\begin{aligned} \dot{V}_1 &= \dot{V}_1 + \dot{V}_2 \\ &\le -m_1 V_1^{\frac{1}{2}} - m_2 V_1^2 + \frac{a}{2} z_2^2 + z_2 \dot{z}_2. \end{aligned} \tag{29}$$

By Substituting $\dot{z}_2$ into (29), we have

$$\begin{aligned} \dot{V}_1 \le &- m_1 V_1^{\frac{1}{2}} - m_2 V_1^2 + \frac{a}{2} z_2^2 \\ &+ z_2(-b x_1 - c x_2 - d + k u - \dot{\beta}). \end{aligned} \tag{30}$$

The control signal u is designed as follows

$$k u = b x_1 + c x_2 + d + \dot{\beta} - m_3 - m_4 z_2^3 - \frac{a}{2} z_2. \tag{31}$$

Substitute (31) into (30) yields

$$\dot V = \dot V_1 + \dot V_2 \le -m_1 V_1^{\frac{1}{2}} - m_2 V_1^2 - m_3 V_2^{\frac{1}{2}} - m_4 V_2^2. \quad (32)$$

By using **Lemma 3**, we have

$$\dot V = (V_1^{\frac{1}{2}} + V_2^{\frac{1}{2}})^2 = V_1 + V_2 + 2(V_1 V_2)^{\frac{1}{2}} \ge V_1 + V_2. \quad (33)$$

Substitute (33) into (32) yields

$$\begin{aligned} \dot V &= \dot V_1 + \dot V_2 \\ &\le -m_1 V_1^{\frac{1}{2}} - m_2 V_1^2 - m_3 V_2^{\frac{1}{2}} - m_4 V_2^2 \\ &\le -m_5 (V_1^{\frac{1}{2}} + V_2^{\frac{1}{2}}) - m_6 (V_1^2 + V_2^2) \\ &\le -m_5 (V_1 + V_2)^{\frac{1}{2}} - m_6 (V_1 + V_2)^2 \\ &(m_5 = \min(m_1, m_3), m_6 = \min(m_2, m_4)). \end{aligned} \quad (34)$$

To sum up, it follows from **Lemma 2**. The proof is completed. The output voltage tracks up to the reference voltage in a fixed time under the action of the controller (31).

4. DESIGN OF THE FINITE TIME CONTROLLER

In this section, according to the finite time control theory, the controller of Buck converter with finite time is designed as comparison. Firstly, the Lyapunov function is constructed. Then the intermediate control rate is designed by the backstepping method. Finally, the suitable u is found to satisfy the finite time control theory.

Theorem 3 For the transformed error system (17), if the controller u is designed as

$$u = \frac{b}{k} x_1 + \frac{c}{k} x_2 + \frac{1}{k} \dot{\bar\beta} + \frac{d}{k} - \frac{a}{2k} z_2 - \frac{m_9}{k}, \quad (35)$$

then the state of the system converges to the origin in a finite time.(Note:$m_{\bar h}$ is positive number($\bar h$ =7,...,12).)

Proof: A backstepping method combined with finite time control theory is employed.

Step 1: In this step, we design the virtual control signal $\bar\beta$ such that $\bar V$ satisfies

$$\dot{\bar V} = \dot{\bar V}_1 + \dot{\bar V}_2 \le -m_8 \bar V_1^{\frac{1}{2}} + \frac{a}{2} z_2^2 + z_2 \dot z_2. \quad (36)$$

We design the Lyapunov functional candidate as

$$\bar V = \bar V_1 + \bar V_2, \quad (37)$$

$$\bar V_1 = \frac{1}{2} z_1^2, \quad (38)$$

$$\bar V_2 = \frac{1}{2} z_2^2. \quad (39)$$

The derivative of (37) is

$$\dot{\bar V} = \dot{\bar V}_1 + \dot{\bar V}_2. \quad (40)$$

The derivative of (38) is

$$\dot{\bar V}_1 = z_1 \dot z_1 = z_1 z_2 a + z_1 a \bar\beta. \quad (41)$$

By **Lemma 4** inequality scaling, we have

$$\dot{\bar V}_1 \le \frac{a}{2} z_1^2 + \frac{a}{2} z_2^2 + z_1 a \bar\beta. \quad (42)$$

The virtual control signal $\bar\beta$ is designed as

$$\bar\beta = -\frac{1}{2} z_1 - m_7. \quad (43)$$

The derivative of (43) is

$$\dot{\bar\beta} = -\frac{1}{2} \dot z_1. \quad (44)$$

By Substituting (43) into (41), we have

$$\begin{aligned} \dot{\bar V} &= \dot{\bar V}_1 + \dot{\bar V}_2 \\ &\le -m_8 z_1 + \frac{a}{2} z_2^2 + z_2 \dot z_2. \end{aligned} \quad (45)$$

By Substituting $\dot z_2$ into (45), we have

$$\begin{aligned} \dot{\bar V} \le &- m_8 \bar V_1^{\frac{1}{2}} + \frac{a}{2} z_2^2 \\ &+ z_2(-b x_1 - c x_2 - d + k u - \dot{\bar\beta}). \end{aligned} \quad (46)$$

Step 2: In this step, we design the u to satisfy the finite time control theorem.

The control signal u is designed as follows

$$k u = b x_1 + c x_2 + d + \dot{\bar\beta} - \frac{a}{2} z_2 - m_9. \quad (47)$$

Substitute (47) into (46) yields

$$\dot{\bar V} = \dot{\bar V}_1 + \dot{\bar V}_2 \le -m_{10} \bar V_1^{\frac{1}{2}} - m_{11} \bar V_2^{\frac{1}{2}}. \quad (48)$$

By using **Lemma 3**, we have

$$(\bar V_1^{\frac{1}{2}} + \bar V_2^{\frac{1}{2}})^2 = \bar V_1 + \bar V_2 + 2(\bar V_1 \bar V_2)^{\frac{1}{2}} \ge \bar V_1 + \bar V_2. \quad (49)$$

Substitute (49) into (48) yields

$$\begin{aligned} \dot{\bar V} &= \dot{\bar V}_1 + \dot{\bar V}_2 \\ &\le -m_{12} (\bar V_1^{\frac{1}{2}} + \bar V_2^{\frac{1}{2}}) \\ &\le -m_{12} (\bar V_1 + \bar V_2)^{\frac{1}{2}} \\ &(m_{12} = \min(m_{10}, m_{11})). \end{aligned} \quad (50)$$

Therefore, it follows from **Lemma 1**.The proof is completed. The output voltage tracks up to the reference voltage in a finite time under the action of the controller (47).

5. SIMULATION AND EXPERIMENT ANALYSIS

In this simulation, the control strategy is shown in Fig 2. The switching frequency of PWM generator is 100kHz.

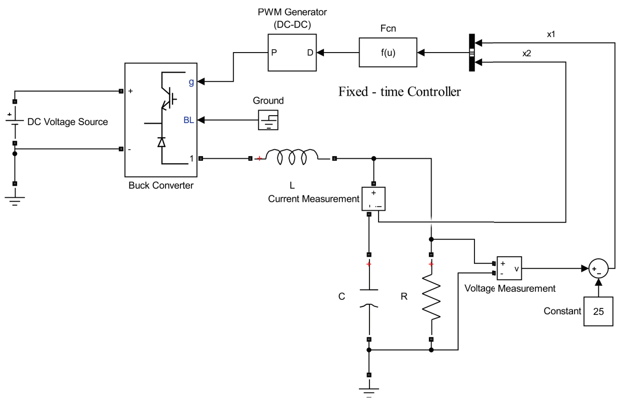

Fig. 2. Simulation circuit based on fixed-time control.

5.1 Selection of simulation circuit parameters

The parameters of three controllers(the parameters of the sliding mode controller are designed according to the method in (Cheng et al., 2020)) and system models are given, as shown in Table 1 and Table 2 below. In order to get the better control effect, the control parameters are obtained by trial and error method.

Table 1. System model parameters

Description	Parameters	Value
Input voltage	V_{in}	50 V
Reference voltage	V_{ref}	25 V
Inductance	L	150 μH
Capacity	C	1000 μF
Rsistance	R	1 Ω

Table 2. Controller model parameters

Fixed-time controller	b/k	c/k	(d-m3)/k	m4/k
Value	-0.01	-6000	-100	-1000
Finite-time controller	b/k	c/k	(d-m8)/k	–
Value	-0.01	-6000	-100	–

5.2 Transient response analysis

The load is kept constant at 1 Ω , and the reference voltage is set at 25 V. In Fig. 3, the tracking results show that the fixed time controller is obviously superior to the finite time controller and sliding mode controller in response speed and steady-state error, and the fixed time controller is stable at about 0.3 ms, while the finite time controller is greater than 8 ms.The sliding mode controller has an obvious chattering.

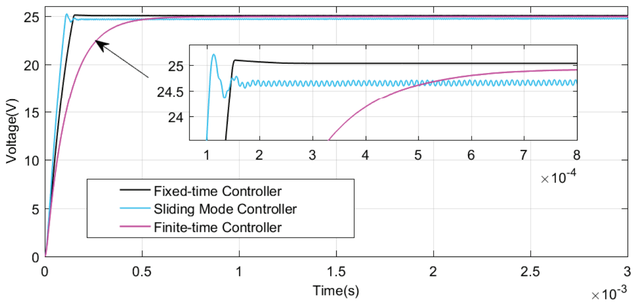

Fig. 3. Comparison of three controllers tracking voltage speed.

We set the reference voltage to change from 25V to 30V in 2 ms , and other parameters remain unchanged. In Fig. 4 , for the dynamic response waveform of the system. it can be seen that the proposed fast fixed time voltage control strategy is obviously superior to the response speed of finite time and sliding mode strategy, in which the stable time of the fixed time control system is at about 2.1 ms and that of sliding mode controller is greater than 2.2 ms . When the reference voltage changes from 25V to 30V, the finite time control system can reach stability only at after 2.6 ms at the beginning of startup. There is a certain gap between the steady-state errors of the three controllers. The steady-state error of the fixed time controller is the smallest of the three. When the load becomes 1.2 Ω at 1 ms, it can be seen from the Fig. 5 that the adjustment time of the proposed fixed time controller is faster than

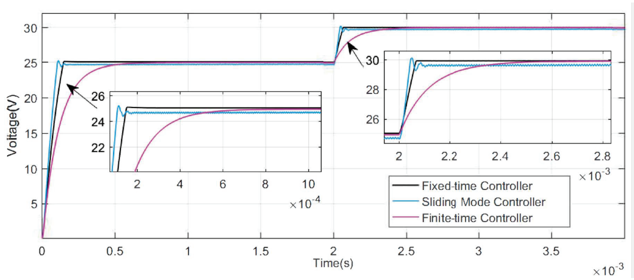

Fig. 4. Tracking speed of the three controllers when the reference voltage changes.

that of the finite time controller and the sliding mode controller. The finite time controller reaches stability at 1.4 ms, while the fixed time controller and the sliding mode controller reach stability before 1.1 ms. Moreover, the error and convergence time of fixed time control are smaller.

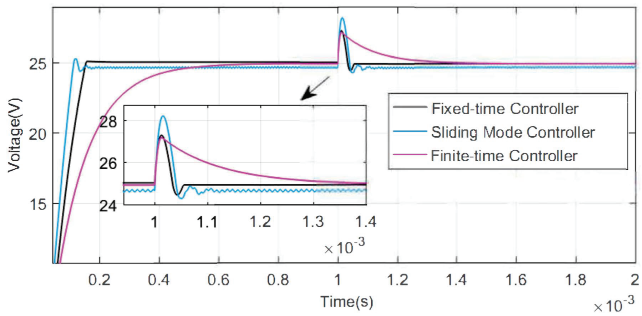

Fig. 5. Comparison of tracking voltages of three controllers under load changes.

5.3 Current ripple analysis

It can be clearly seen from Fig. 6 that there is a big gap between sliding mode controller and the other two controllers. Compared with finite time controller and fixed time controller, sliding mode controller has a larger ripple current (the amplitude is about 0.4A). In Fig. 7, it can be seen that effect of ripple suppression of fixed time controller is the best, and the ripple amplitude is the smallest. The current ripple of the circuit with the finite time controller is close to that of the fixed time controller. Therefore, the proposed fixed time Buck control method is effective against suppressing current ripple and has smaller current fluctuation.

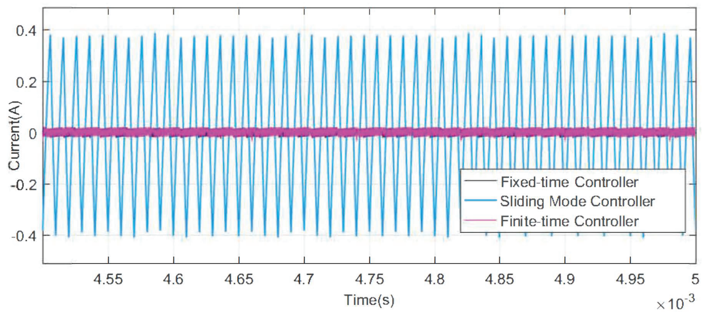

Fig. 6. Comparison of current ripple under three controllers.

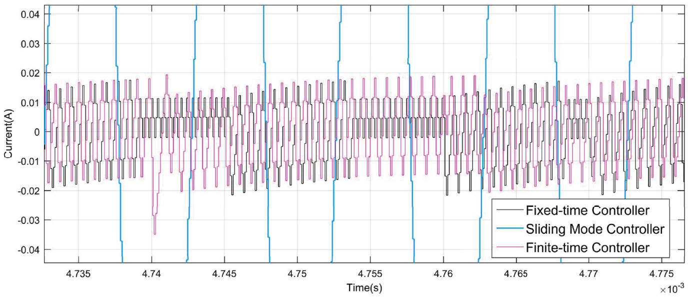

Fig. 7. Comparison of current ripple details between fixed-time controller and finite-time controller.

5.4 Experiments Results with the Buck circuit system

Hardware circuit (as shown in Fig. 9) consists of Buck circuit, voltage and current sampling circuit and control circuit composed of DSP28335 main control board. The input voltage is 40V and the resistance is 25 Ω, the set voltage is 25V. In order to facilitate the early debugging, the control software platform, Buck circuit control interface (as shown in Fig. 8), is designed in PC, and communicates with DSP through 485 serial port. The whole design framework (as shown in Fig. 10) and the control strategy are downloaded to the DSP board. The DSP outputs PWM wave to the driving circuit, and the driving circuit to the Buck circuit. The current and voltage information of the main circuit can be collected through the sampling circuit.

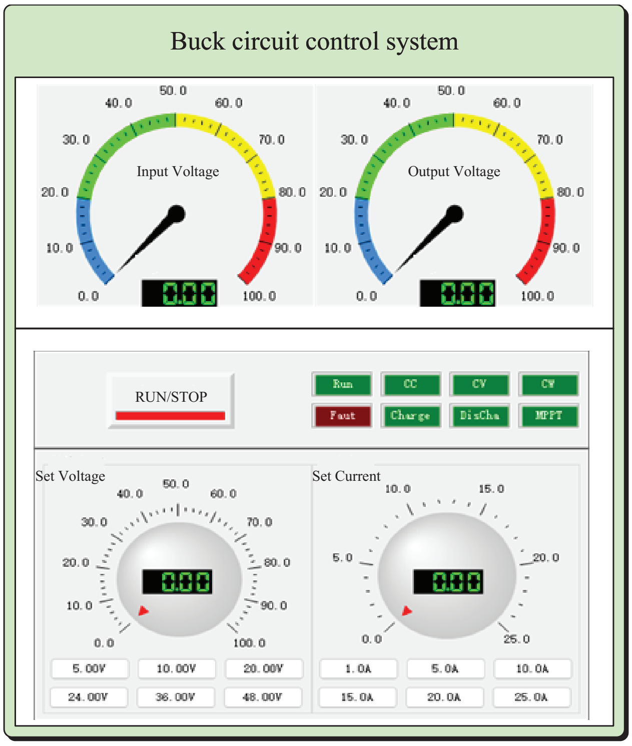

Fig. 8. Buck circuit control system in PC

As shown in Fig. 11 and Table 3, the overshoot of the proposed strategy is much smaller than that of the finite time controller and the sliding mode controller. The settling time with the proposed strategy is shortened by 14% compared with that of the finite time control and 24% compared with that of the sliding mode control.

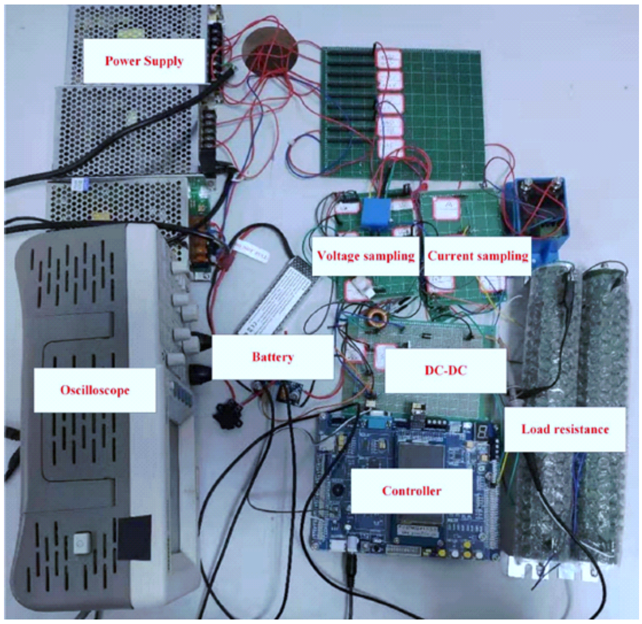

Fig. 9. Hardware test platform

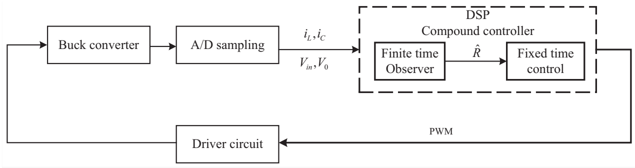

Fig. 10. Hardware block diagram

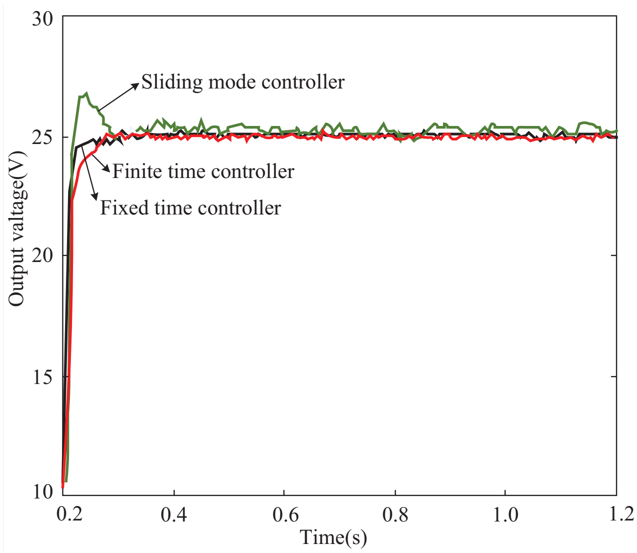

Fig. 11. Comparison of three controllers at set voltage 25V

The simulation and experiment results show that, the composite controller combining a fixed time controller with a finite time observer has advantages in convergence speed and interference resistance, the reason of which is the convergence time of fixed time controller does not depend on the initial state. Meanwhile, the load observer can accurately and quickly track the load changes. This can be well reflected on Buck converter when the load and reference voltage changes. Hence, the fixed time controller based on load finite time observer can track reference

Table 3. Comparisons under Sliding mode controller, Finite time controller and Fixed time controller

Controller	Overshoot(V)	Settling Time(ms)
Sliding mode controller	2.1	365.6
Finite time controller	0.5	323.1
Fixed time controller	0.2	276.8

voltage quickly and reduce current ripple, which has been verified in convergence speed and anti-interference.

6. CONCLUSIONS

This paper proposes a fixed time voltage regulation control strategy based on load finite time observer to improve the transient response of the Buck converter and also to reduce the current ripple in the circuit. Fixed time controller combined with a finite time observer is designed instead of the traditional method of adding additional circuits and sliding mode control to improve the stability and fast response of the system. By constructing a Lyapunov function, the fixed time stability has been proved. Simulation results have shown that the output voltage can track the reference voltage in a fixed time. Compared with the sliding mode controller and finite time controller, the Buck converter with fixed time controller has faster transient and smaller current ripple when the load and reference voltage changes.

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